

Application Note **AN-11001**

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| Prepared by: | Ingo Staudt |

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3L NPC & TNPC Topology

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This application note provides information on two three level topologies: the three level NPC (3L NPC; **N**eutral **P**oint **C**lamped) and the three level TNPC (3L TNPC; **T**-type **N**eutral **P**oint **C**lamped). The reader will gain insight in elementary thoughts of how these 3L devices work; where advantages and disadvantages are. Some hints concerning the layout/setup of 3L modules are given as well. However, the information given is not exhaustive and the responsibility for a proper design remains with the user.

General

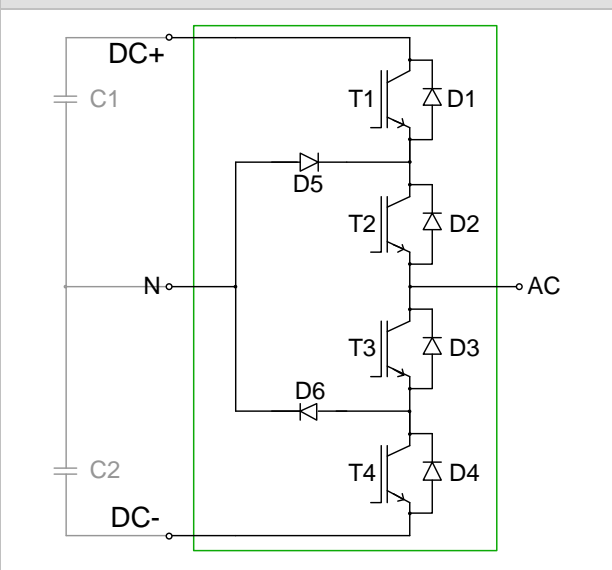
One benefit of using 3L NPC or 3L TNPC topology is the lower current THD; that reduces the filtering effort (less copper needed, lower losses in the filter).

A major advantage of 3L NPC is the possibility to use IGBTs and diodes with breakdown voltages that are lower than the actual DC-link voltage. The lower blocking

devices produce lower losses and so the efficiency can be increased. By using the same blocking voltage as in a 2L applications higher DC-link voltages can be realized.

Compared to a 2L phase leg module one phase leg of a 3L NPC module consists of 10 instead of 4 semiconductors (Fig. 1): 4 **I**GBTs (T1 - T4), 4 antiparallel **F**ree-**W**heeling **D**iodes (FWD; D1 - D4) and 2 **C**lamping **D**iodes (CD; D5 and D6).

Fig. 1: Green box: content of a 3L NPC phase leg

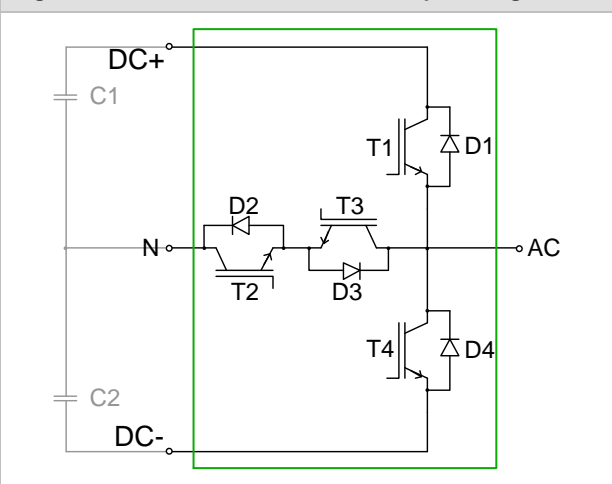


Four power terminals connect the module to AC and to the DC-link: DC+, DC- and N (neutral). The DC-link is split in two symmetric halves connected in series; the upper half connecting DC+ and N and the lower half connecting N and DC-.

In this 3L topology every conduction path consists of two semiconductors in series and it can either handle higher DC-link voltages or the blocking voltage of the switches can be reduced in comparison to a 2L topology.

The benefit of 3L TNPC is the 3L output voltage waveform while there are no restrictions to the switching scheme as in 3L NPC (especially in emergency shutdown).

Fig. 2: Green box: content of a 3L TNPC phase leg



A 3L TNPC phase leg (Fig. 2) consists of only 8 semiconductors: 4 IGBTs (T1 - T4) and 4 antiparallel Free-Wheeling Diodes (FWD; D1 - D4). As a 3L NPC the TNPC is connected to the split DC-link at DC+, N and DC-. The fourth power terminal provides the AC output. In 3L TNPC topology semiconductors with different breakdown voltages are used: T1 and T4 (which are referred to as *outer* switches) need to withstand the full

DC-link voltage. The *inner* switches (indices 2 and 3) connect AC to Neutral and must be able to block half of the DC-link voltage.

In 3L TNPC topology the conduction paths are either through one higher blocking semiconductor (outer switch) or two lower blocking devices in series (inner switches).

Naming the semiconductors as shown in Fig. 1 and Fig. 2 inherits the advantage that the exact same switching pattern can be used for both 3L NPC and 3L TNPC topology.

Difference 2L ↔ 3L

The difference between 2L and 3L topology is not only the number of semiconductor devices. While the well-known 2L converter switches either DC+ or DC- to the AC terminal (Fig. 3), the 3L versions connect the AC either to DC+, DC- or N. N(utral) is the midpoint voltage between DC+ and DC- and forms the third voltage level where the three level topology has its name from.

Fig. 3: Voltage and current waveforms of 2L

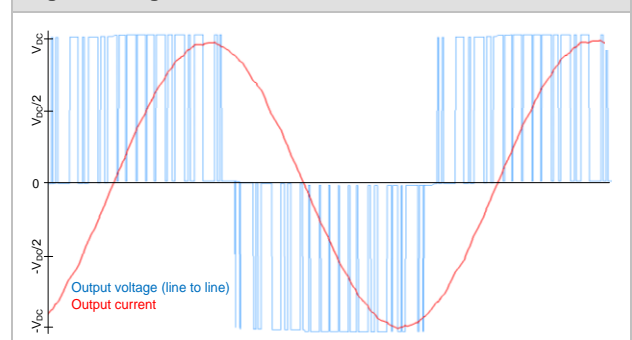
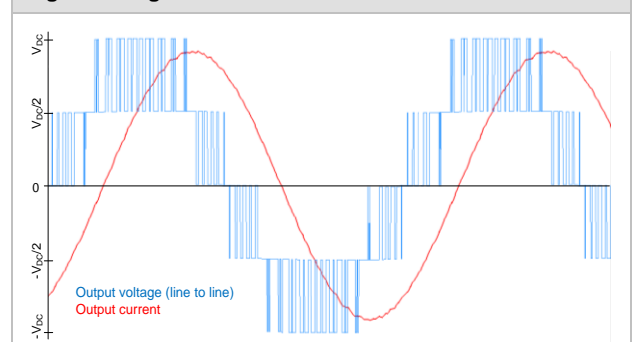


Fig. 4: Voltage and current waveforms of 3L



By introducing a third voltage level the waveform of the output voltage is approximated closer to the desired sine waveform (Fig. 4) and the current THD can be reduced. Thus strong requirements concerning grid quality (when feeding to the grid) can be met more easily.

Comparison of 2L ↔ 3L NPC/TNPC:

NPC & TNPC:

- For reaching the same current THD value with 3L topology the switching frequency can be

reduced leading to reduced switching power losses.

- Subsequently operation at a working point producing the same switching frequency as in 2L topology the current THD can be reduced in 3L topology.
- In 3L applications the switching frequency can be reduced compared to 2L applications, still improving the THD and reducing the filtering effort.
- As the number of IGBTs has increased from 2 to 4 also the number of gate drivers increases. The auxiliary power consumption grows as well as the control effort.

NPC:

- The number of switches in the active current path in 3L NPC topology is doubled; that increases the conduction power losses.
- In 3L NPC applications semiconductors with a lower blocking voltage capability may be used; example: DC-link voltage of 750V can be handled with 1200V 2L or 650V 3L modules (each switch only needs to block 375V). The lower losses of the lower blocking devices compensate the additional losses due to the increased number of devices in the current path.
- The maximum DC-link voltages are 800V_{DC} using 650V semiconductors, 1500V_{DC} using 1200V semiconductors and 2400V_{DC} using 1700V semiconductors.

TNPC:

- The number of switches in the active current path in 3L TNPC topology is either similar to 2L (outer switches) producing the same losses or doubled (with lower blocking voltage; inner switches) leading to higher conduction but lower switching losses.
- The maximum DC-link voltages are as for a 2L module: 400V_{DC} using 650V semiconductors, 800V_{DC} using 1200V semiconductors and 1200V_{DC} using 1700V semiconductors.

Switching pattern of a 3L converter

The control of 3L applications is more sophisticated than 2L. While the 2L switching pattern is pretty simple (TOP and BOT IGBTs always switch inversely) it gets more complicated at 3L as certain switches (namely T2 and T3) are switched on for quite a while depending on the value of $\cos \varphi$ (up to a half period for $\cos \varphi = 1$). The number of possible switching states increases from 4 in 2L topology (TOP/BOT: 0/0, 0/1, 1/0, 1/1) to 16.

At 3L NPC a distinction is drawn between allowed, potentially destructive and destructive states (Fig. 5).

Fig. 5: Switching states NPC

| | | | | | | | | | | | | | | | | |
|-------|---------|---|---|---|---|---|-------------------------|---|---|---|-------------|---|---|---|---|---|
| T1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| T2 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| T3 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| T4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| state | allowed | | | | | | potentially destructive | | | | destructive | | | | | |

Allowed states:

- All IGBTs are in off-state; the converter is switched off.
- Either T2 or T3 may be switched on solely.
- Each state where two adjacent IGBTs are switched on (T1/T2, T2/T3, T3/T4).

Potentially destructive states:

- Either T1 or T4 is switched on solely or together.
- Two not adjacent IGBTs are switched on (T1/T3 or T2/T4).

The consequences depend on the switching pattern applied to the modules of the other phase legs.

Destructive states:

- Three adjacent IGBTs are switched on (T1/T2/T3 → shorting upper half of DC-link; T2/T3/T4 → shorting lower half of DC-link)
- Three not adjacent IGBTs are switched on (T1/T2/T4 → full DC-link voltage applies to T3; T1/T3/T4 → full DC-link voltage applies to T2)
- Four IGBTs switched on → DC+, DC- and N shorted.

At 3L TNPC the distinction is drawn only between allowed and destructive states (Fig. 6).

Fig. 6: Switching states TNPC

| | | | | | | | | | | | | | | | | |
|-------|---------|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|
| T1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| T2 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| T3 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| T4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| state | allowed | | | | | | | | destructive | | | | | | | |

Allowed states:

- All IGBTs are in off-state; the converter is switched off.
- Any one of the IGBTs may be switched on solely.
- Each state where two adjacent IGBTs are switched on (T1/T2, T2/T3 or T3/T4).

Destructive states:

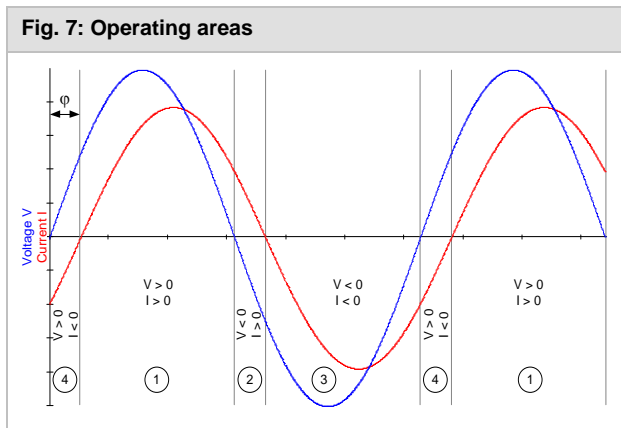
- Two not adjacent IGBTs are switched on (T1/T3 → shorting upper half of DC-link; T2/T4 → shorting lower half of DC-link; T1/T4 → shorting DC+ and DC-).

- Three not adjacent IGBTs are switched on (same consequences as above: shorting either upper half or lower half or the full DC-link)
- Four IGBTs switched on → DC+, DC- and N shorted.

Commutations and commutation paths

NPC & TNPC:

Fig. 7 shows a sine voltage (blue trace) and the related current (red trace) at inductive load. The inverter operation can be divided in four operating areas. For $\cos \varphi = +1$ (no phase shift) voltage and current waveforms are in phase; only working areas 1 and 3 are active. For $\cos \varphi = -1$ (180° phase shift) only working areas 2 and 4 are active.



For any value of $\cos \varphi$ between -1 and +1 the phase shift changes and so do the time shares of the four working areas.

The active switches and the commutations for these four working areas are listed below:

- both voltage and current are greater than 0 ($V > 0, I > 0$):
 - 2L: $T_{TOP} \leftrightarrow D_{BOT}$
 - 3L NPC: $T1/T2 \leftrightarrow D5/T2$ (*short commutation path*)
 - 3L TNPC: $T1 \leftrightarrow D3$
- voltage is less and current is greater than 0 ($V < 0, I > 0$):
 - 2L: $T_{TOP} \leftrightarrow D_{BOT}$
 - 3L NPC: $D5/T2 \leftrightarrow D3/D4$ (*long commutation path*)
 - 3L TNPC: $T2/D3 \leftrightarrow D4$
- both voltage and current are less than 0 ($V < 0, I < 0$):
 - 2L: $T_{BOT} \leftrightarrow D_{TOP}$
 - 3L NPC: $T3/T4 \leftrightarrow T3/D6$ (*short commutation path*)
 - 3L TNPC: $T4 \leftrightarrow T3/D2$

- voltage is greater and current is less than 0 ($V > 0, I < 0$):

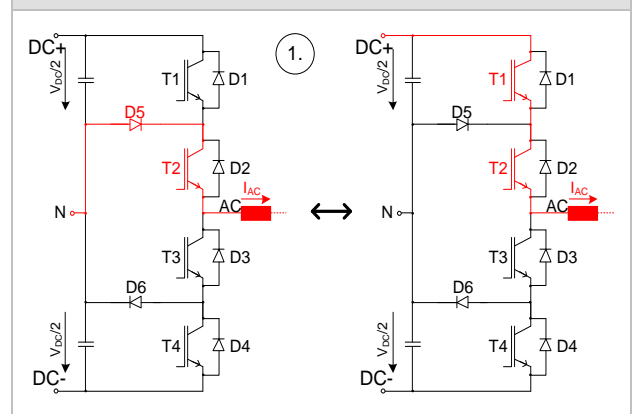
- 2L: $T_{BOT} \leftrightarrow D_{TOP}$
- 3L NPC: $T3/D6 \leftrightarrow D1/D2$ (*long commutation path*)
- 3L TNPC: $T3/D2 \leftrightarrow D1$

NPC:

While in a “short commutation path” the commutation affects only one of the two active switches (e.g. $T1 \leftrightarrow D5$) the current through the other active switch does not change (e.g. $T2$). In a “long commutation path” (e.g. $D5/T2 \leftrightarrow D3/D4$) both devices are affected.

The name “short/long commutation path” also indicates the geometric length of the commutations; while the short commutation takes place either within the upper or the lower half of the 3L module in a long commutation the current changes from the upper to the lower half (or vice versa).

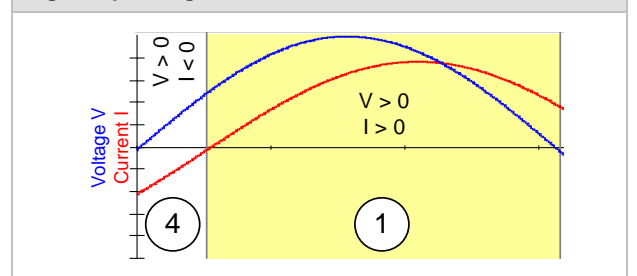
Fig. 8: Short commutation path in operating area 1



The short commutation (Fig. 8) in the upper half of the module (device indices 1, 2 and 5) is active in operating area 1 (Fig. 9); both voltage and current are positive.

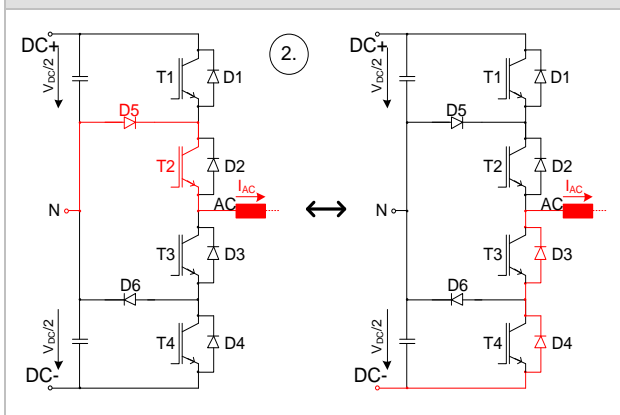
The commutation goes back and forth between $T1$ and $D5$; the current flows from DC+ via $T1$ and $T2$ to the AC terminal as long as $T1$ is switched on. When $T1$ switches off, the current commutates to the clamping diode $D5$; now the current flow is from N via $D5$ and $T2$ to AC. $T2$ stays switched on all the time.

Fig. 9: Operating area 1



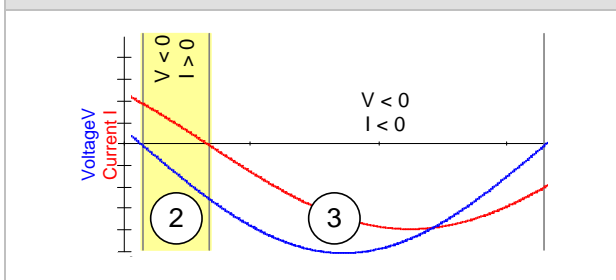
The long commutation for positive output current (Fig. 10) goes back and forth between $D5/T2$ in the upper half of the module and $D3/D4$ in the lower half => across the entire device.

Fig. 10: Long commutation path in operating area 2



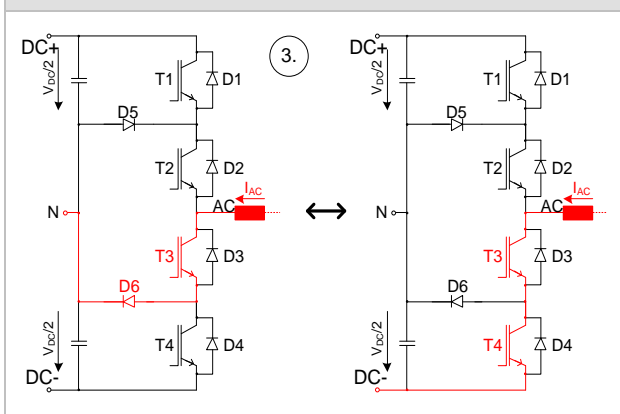
This commutation across the entire device is due to the fact that in operating area 2 (Fig. 11) the current is still positive (flowing from the DC-link towards the load) while the output voltage is negative.

Fig. 11: Operating area 2



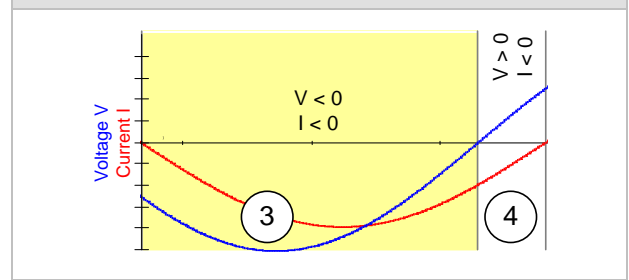
The other short commutation path is active in operating area 3 (Fig. 12 & Fig. 13), in the lower half of the module. Output current and voltage are negative.

Fig. 12: Short commutation path in operating area 3



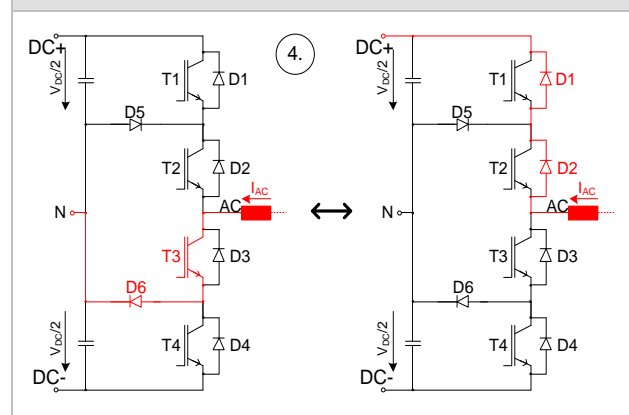
The commutation goes back and forth between T4 and D6; the current flows from the AC terminal across T3 and T4 to DC- as long as T4 is switched on. As soon as T4 switches off, the current commutates to the clamping diode D6; the new conduction path is from AC via T3 and D6 to N. T3 stays switched on all the time.

Fig. 13: Operating area 3



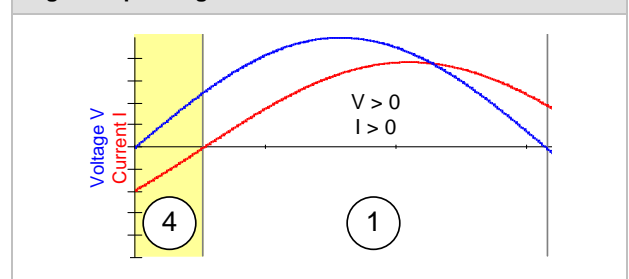
The long commutation path for negative current (Fig. 14) goes back and forth between D6/T3 in the lower half of the module and D1/D2 in the upper half across the entire device.

Fig. 14: Long commutation path in operating area 4



The long commutation in operating area 4 (Fig. 4) comes with negative output current (flowing from the AC terminal towards the DC-link) and positive voltage.

Fig. 15: Operating area 4



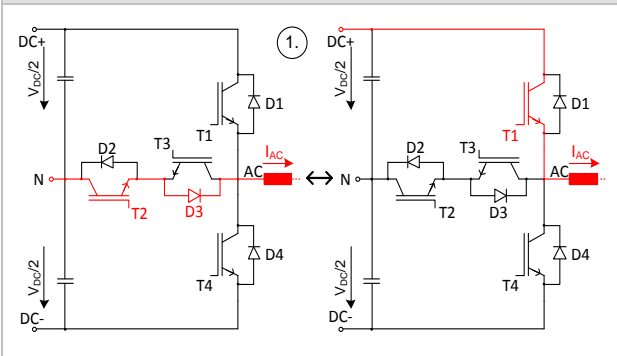
TNPC:

There are no “short” or “long” commutation paths in TNPC topology; all paths are of the same geometric length and inherit one outer switch (indices 1 or 4; either IGBT or diode) and two inner switches (either T2 and D3 or T3 and D2). In normal operation the commutation always affects one outer and two inner switches; there is no commutation between T1/D1 and T4/D4.

In operating area 1 (Fig. 16 & Fig. 9) output voltage and current are positive, the current flows towards the AC terminal. The commutation goes back and forth between T1 and T2/D3; the current flows from DC+ via T1 to the AC terminal as long as T1 is switched on. When T1

switches off, the current commutates to the inner switches T2/D3; the current now flows from N via T2 and D3 to AC. T2 stays switched on all the time; as soon as T1 is switched on, the diode D3 blocks the voltage and so avoids a short cut of the upper half of the DC-link.

Fig. 16: Commutation path in operating area 1



In operating area 2 (Fig. 17) the output current is still positive while the voltage is negative (Fig. 11). It commutates back and forth between the inner switches T2/D3 and the diode D4.

Fig. 17: Commutation path in operating area 2

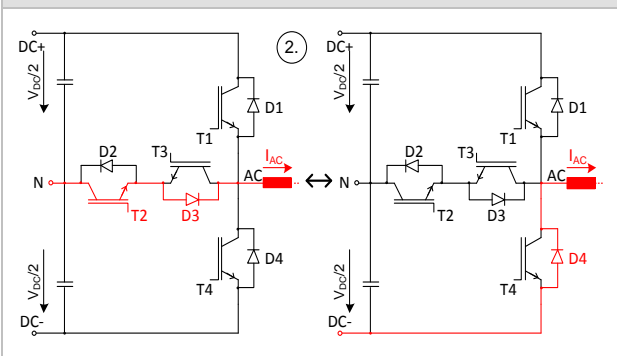
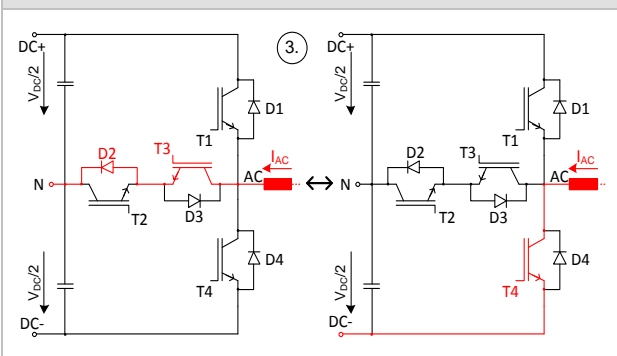


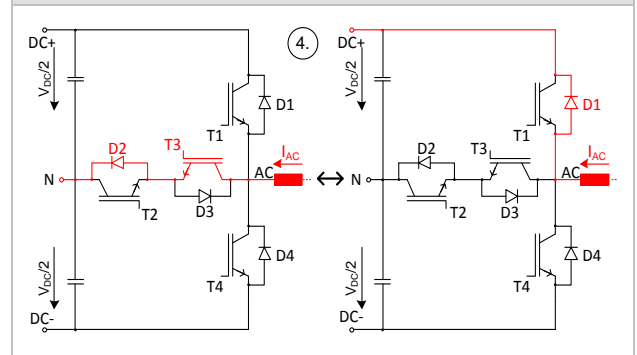
Fig. 18 shows the conduction paths of operating area 3; the current commutates between T4 and the inner switches T3/D2. The current flows from the AC terminal to the DC-link and, current and voltage are negative (see Fig. 13). T3 stays switched on permanently; as long as T4 is switched on as well the diode D2 blocks the voltage and avoids shorting the negative half of the DC-link.

Fig. 18: Commutation path in operating area 3



In operating area 4 (Fig. 19) the output current is negative while the voltage is positive (Fig. 15). The current commutates back and forth between the inner switches T3/D2 and the diode D1.

Fig. 19: Commutation path in operating area 4



3L converter

Module consideration

When a 3L module is designed especially the commutation paths find consideration: large commutation paths inherit large stray inductances. When the load current through a conduction path with large stray inductance is switched off high voltage overshoots occur. To avoid a destruction of the semiconductor the voltage overshoot must stay below its blocking voltage. That can be reached by either reducing the maximum allowed DC-link voltage and allowing higher overshoots or by reducing the stray inductances producing less overshoots.

Of course the aim is to reduce the stray inductance and allow higher DC-link voltages (that increases the possible AC output voltage and so the module power).

Setup with standard 2L modules

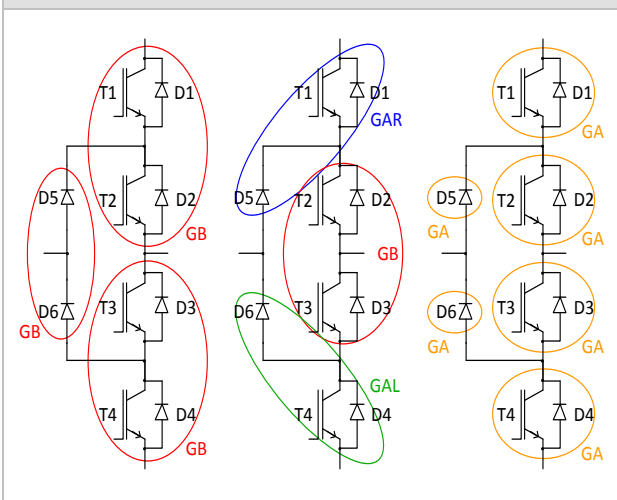
Theoretically 3L topologies can be set up with already existing standard 2L modules (Fig. 20 & Fig. 21). The assembly would require bus bar interconnection of the modules and would be very scalable.

NPC:

Practically the NPC setup from 2L modules (Fig. 20) inherits always very long conduction paths, especially for the commutations across module borders (that gets even worse for the long commutation paths).

Due to the stray inductance these large commutation paths produce very high voltage overshoots so that the shown setups offer no advantages in regard to 2L designs.

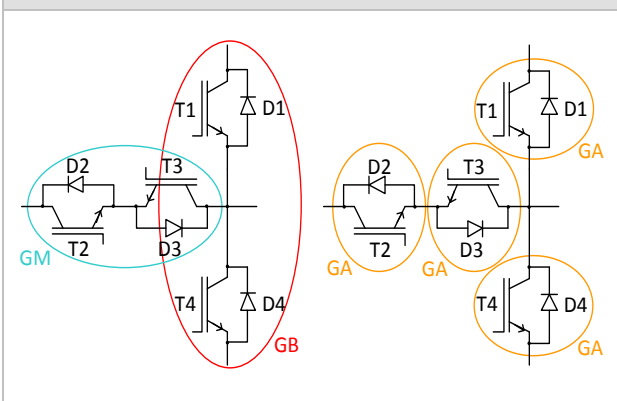
Fig. 20: 2L configurations to set up a 3L NPC module



In the TNPC setup from 2L modules (Fig. 21) every commutation path is across module borders. Similar to the NPC setup stray inductances lead to high voltage overshoots which make this solution unattractive.

TNPC:

Fig. 21: 2L configurations to set up a 3L TNPC module



Dedicated 3L modules

As the 3L topology setup from 2L modules appears not to be the best solution a new module design has been made facing the special requirements coming with the 3L technology.

At the very beginning a choice must be made concerning the module size and the related electric module power: the bigger the module shall become the more power it can provide as large chip area is available. Unfortunately larger module size also stands for higher stray inductances leading to high switching voltage overshoots thus limiting the maximum current.

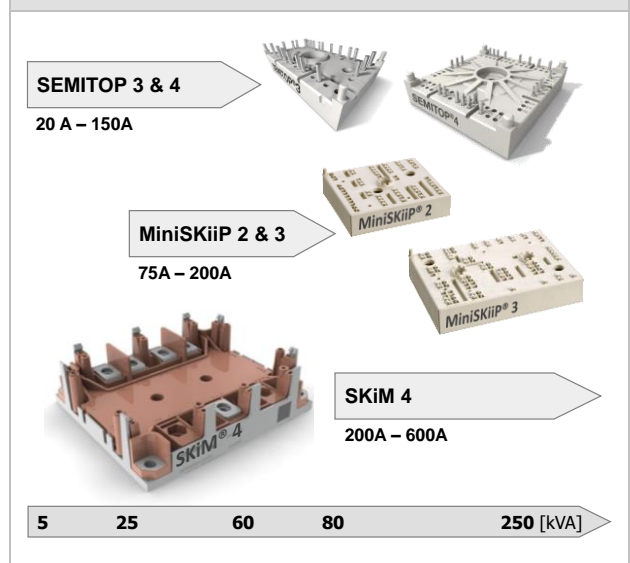
High power can either be realized by one large module or by many smaller modules in parallel. The latter solution requires an equally high number of driving units that need to be parallelized (with known problems: cost, space, jitter of separate drivers, compensation current when using paralleled drivers...).

SEMIKRON 3L modules

SEMIKRON provides a number of 3L modules that have been specially redesigned to minimize stray inductance. The module range starts with SEMITOP at a rated chip current of 20A to 150A followed by MiniSKiiP (75A - 200A) up to SKiM modules with 200A - 600A rated current. While SEMITOP and MiniSKiiP are available for DC-link voltages of up to approx. 800V, SKiM modules allow for up to 1500V. The output power range goes as far as 250kVA (Fig. 22).

As soon as even higher power is required several modules need to be connected in parallel.

Fig. 22: SEMIKRON 3L module portfolio



The major benefit of the 1200V NPC module is that a maximum AC output voltage of 1000V can be realised at 1500V DC-link. So it is possible to stay right within the low voltage directive (harmonised standards apply) on the one hand and reduce the converter current on the other without a change to the output power.

Driving 3L devices

Normal operation sequences

NPC & TNPC:

When all devices are switched off and the 3L converter starts operation it must be one of the inner IGBTs to be switched on first. In case of positive output voltage that is T2. After a short while (when T2 is entirely switched on) T1 may be pulsed. For the switch-off sequence the reverse order must be maintained: it must be made sure that T1 is thoroughly switched off before T2 may be turned off. That can be achieved by turning off T2 a short time (1..3µs) after the turn-off signal for T1 has occurred; this dead time is well known as interlock-time between TOP and BOT switch at SEMIKRON 2L gate drivers.

NPC:

When an inner IGBT (T2 or T3) is switched off before the corresponding outer IGBT (T1 or T4) the inner switch would be exposed to the full DC-link voltage. In case this voltage was higher than the blocking voltage of that semiconductor it would be destroyed.

As shown in Fig. 5 there are switching patterns that are not allowed because they are destructive. Those states must be avoided if the device shall not be destroyed.

TNPC:

The same rules as stated for NPC also apply for TNPC converters. When an inner IGBT (T2 or T3) is switched off before the corresponding outer IGBT (T1 or T4) the load current would commute from an outer IGBT (T1 or T4) to an outer diode (D4 or D1). This commutation path inherits a higher inductance and thus the outer IGBT switching off would be exposed to a higher voltage overshoot. In case this overshoot exceeded the blocking voltage of that semiconductor it would be destroyed.

Subsequently turning off in different order or turning off all IGBT simultaneously is only possible when the semiconductors' blocking voltages are not exceeded.

As shown in Fig. 6 there are switching patterns that are not allowed because they are destructive. Those states must be avoided if the device shall not be destroyed.

NPC & TNPC:

The gate signals of T1 and T3 (T2 and T4 respectively) are inverses. It has to be made sure that one IGBT is securely switched off before the other one is switched on.

Emergency shut-down

There are several events that may occur which in 2L application lead to immediate switch-off by the driver to protect the semiconductors. Imaginable events are:

- thermal overload
- current overload or
- desaturation.

Any of these scenarios must lead to a quick shut-down in 3L application as well.

NPC & TNPC:

But it must be made sure that the correct switch-off sequence is maintained: outer IGBT first (T1 or T4), inner IGBT afterwards (T2 or T3) to avoid destruction due to voltage breakdown.

Where thermal overload or a slowly rising current can be monitored with NTC/PTC and current sensors and leave some time for the supervising controller to react in an appropriate time, a desaturation event leaves a maximum of 10µs time for switch-off.

When an outer switch (T1 or T4) desaturates it may be switched off immediately by the driver. Within 1..3µs the according inner IGBT is to be switched off as well.

It gets more complicated, when the desaturation happens at an inner switch (T2 or T3): when the event is

monitored the driver must have the information if an according outer switch is switched on as well or not. If it is switched on the gate driver must switch off the outer IGBT immediately, wait 1..3µs and then switch off the inner IGBT as well. If no outer IGBT is switched on the driver must switch off the inner IGBT immediately.

In any case the driver generates an error message so that the controller can shut down the other devices of the converter as well and so establish a secure state.

Protection of 3L devices against voltage overshoots

As soon as a current path is interrupted (by switching off an IGBT or a diode) the voltage across the switched off device begins to rise. This voltage overshoot is caused by the energy stored as magnetic field of the current path. The energy increases linearly with rising stray inductance L_S ($E = 0.5 \cdot L_S \cdot i^2$); e.g. doubled parasitic inductance L_S causes doubled energy E . The voltage overshoot ($V = L_S \cdot di/dt$) is added to the DC-link voltage; the sum must not exceed the blocking voltage of the semiconductor as it would be destroyed.

Due to the fact that a 3L module is larger than a 2L device and a conduction path inherits two switches the current paths are longer and hence the stray inductances higher. Especially the long commutation paths (NPC topology; T2/D5 \leftrightarrow D3/D4 or T3/D6 \leftrightarrow D1/D2) must be paid attention to when the module is designed.

While with a good design low values of the stray inductances can be realised (e.g. SKiM4 MLI: 28nH per switch, approx. 60nH for the long commutation path) it is not possible to construct a low inductive 3L setup with standard 2L modules. The long commutation path passes at least three modules in NPC topology (see Fig. 20) or two of three modules in TNPC topology (Fig. 21) what leads to a stray inductance of about 200nH. That is more than three times as much as in the dedicated 3L module. Assuming the di/dt is the same this setup produces more than three times as much voltage overshoot.

For that reason SEMIKRON recommends the use of dedicated 3L modules.

If there are no further possibilities to reduce the voltage overshoot at its root cause (i.e. even shorter connections between the semiconductors which at a certain point is not possible any more) the overshoot needs to be handled in a way protecting the semiconductors.

Snubber

Snubber capacitors can be connected to DC+ and N respectively N and DC-. They must be positioned as close to the module as possible and can be chosen according to the hints given in SEMIKRON Application Note AN-7006.

Active Clamping

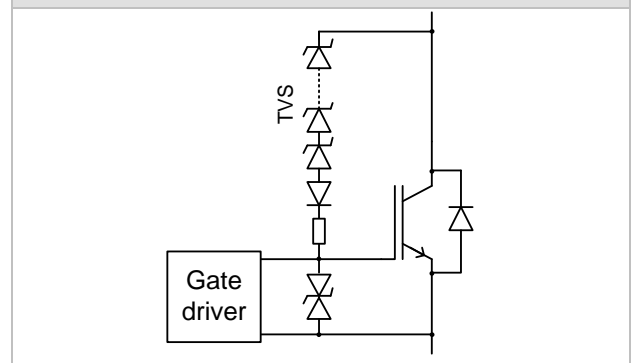
Another way to handle harmful voltages is to use an active clamping network at the IGBTs (Fig. 23).

This network consists of several in series connected transient voltage suppressor (TVS) diodes providing a breakdown voltage which is slightly below the IGBT's breakdown voltage. The clamping network is connected between collector and gate of the device that shall be protected.

When the switch is turned off and the voltage across increases above the breakdown voltage of the TVS diodes they start conducting a current into the gate of the IGBT. The IGBT starts conducting as well; that leads to a voltage breakdown across the device as soon as the energy stored as magnetic field is exhausted, the TVS

diodes go into blocking mode again and the IGBT switches off.

Fig. 23: Simple active clamping circuit



3L loss calculation

For choosing a 3L module that is best suited for a certain application it is necessary to calculate the power losses that emerge in the different semiconductors. Subsequently the equations for calculating the power losses in 3L NPC and 3L TNPC are shown.

NPC:

The power losses of the 10 semiconductors in 3L NPC topology can be calculated according to:

- **T1 & T4:**

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \left\{ 3V_{ce0} \cdot [(\pi - \varphi) \cdot \cos(\varphi) + \sin(\varphi)] + 2r_{ce}\hat{I} \cdot [1 + \cos(\varphi)]^2 \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 + \cos(\varphi)] \right) \cdot G_I$$

- **T2 & T3:**

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \left\{ V_{ce0} \cdot [12 + 3M(\varphi \cos(\varphi) - \sin(\varphi))] + r_{ce}\hat{I} \cdot [3\pi - 2M(1 - \cos(\varphi))^2] \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 - \cos(\varphi)] \right) \cdot G_I$$

- **D5 & D6:**

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \left\{ V_{f0} \cdot [12 + 3M((2\varphi - \pi)\cos(\varphi) - 2\sin(\varphi))] + r_f\hat{I} \cdot [3\pi - 4M(1 + \cos^2(\varphi))] \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 + \cos(\varphi)] \right) \cdot G_I$$

- D1 & D4:

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \left\{ 3V_{f0} \cdot [-\varphi \cos(\varphi) + \sin(\varphi)] + 2r_f \hat{I} \cdot [1 - \cos(\varphi)]^2 \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 - \cos(\varphi)] \right) \cdot G_I$$

- D2 & D3:

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \left\{ 3V_{f0} \cdot [-\varphi \cos(\varphi) + \sin(\varphi)] + 2r_f \hat{I} \cdot [1 - \cos(\varphi)]^2 \right\}$$

$$P_{sw} = 0$$

TNPC:

The power losses of the eight semiconductors in 3L TNPC topology are different from those of 3L NPC and can be calculated as follows:

- T1 & T4:

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \left\{ 3V_{ce0} \cdot [(\pi - \varphi) \cdot \cos(\varphi) + \sin(\varphi)] + 2r_{ce} \hat{I} \cdot [1 + \cos(\varphi)]^2 \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 + \cos(\varphi)] \right) \cdot G_I$$

- T2 & T3:

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \left\{ V_{ce0} \cdot [12 + 6M(\varphi \cos(\varphi) - \sin(\varphi)) - 3M\pi \cos(\varphi)] + r_{ce} \hat{I} \cdot [3\pi - 4M(1 + \cos^2(\varphi))] \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 - \cos(\varphi)] \right) \cdot G_I$$

- D2 & D3:

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \left\{ V_{f0} \cdot [12 + 3M(2\varphi \cos(\varphi) - 2\sin(\varphi)) - 3M\pi \cos(\varphi)] + r_{ce} \hat{I} \cdot [3\pi - 4M(1 + \cos^2(\varphi))] \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 + \cos(\varphi)] \right) \cdot G_I$$

- D1 & D4:

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \left\{ 3V_{f0} \cdot [-\varphi \cos(\varphi) + \sin(\varphi)] + 2r_f \hat{I} \cdot [1 - \cos(\varphi)]^2 \right\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}} \right)^{K_V} \cdot \left(\frac{1}{2\pi} [1 - \cos(\varphi)] \right) \cdot G_I$$

NPC & TNPC:

The equations are valid for $M = 0 \dots 1$. The modulation index M correlates DC-link voltage and RMS voltage:

$$M = \frac{\sqrt{2} \cdot V_{RMS}}{\sqrt{3} \cdot V_{DC} / 2}$$

Typical values of K_V , K_I and G_I for SEMIKRON modules are shown in Fig. 16.

Fig. 16: Typ. K_V , K_I and G_I values for SEMIKRON modules

| | IGBT | Diode |
|-------|------|-------|
| K_V | 1.4 | 0.6 |
| K_I | 1 | 0.6 |
| G_I | 1 | 1.15 |

SemiSel

SemiSel is SEMIKRON's online simulation tool to calculate losses and temperatures of power semiconductors in customer specific applications. From specific values for cooling (e.g. type and performance of the heatsink, ambient temperature) and electric parameters (e.g. input/output voltage, switching frequency, load current, etc.) SemiSel calculates the power losses and junction temperatures of all IGBTs and diodes within a few seconds. By changing certain parameters the optimum setup (which type of module, switching frequency,...) can easily be found. SemiSel 4.0 has been extended to calculate the 3L NPC topology in the same convenient way as 2L designs.

Symbols and Terms used

| Letter Symbol | Term |
|----------------|---|
| 2L | Two level |
| 3L | Three level |
| CD | Clamping Diode |
| $\cos \varphi$ | Power factor |
| CS1 | Collector Sense of IGBT 1 |
| DC+ | Positive potential (terminal) of a direct voltage source |
| DC- | Negative potential (terminal) of a direct voltage source |
| di/dt | Rate of rise and fall of current |
| E | Electrical energy |
| E_{SW} | Sum of energy dissipation during turn-on and turn-off-time |
| f_{SW} | Switching frequency |
| FWD | Free Wheeling Diode |
| GA | Single Switch |
| GAL | Chopper, low IGBT |
| GAR | Chopper, high IGBT |
| GB | Half-bridge |
| G_I | Adaptation factor for the non-linear semiconductor characteristics |
| GM | Half-bridge with anti-serial switches (IGBT and antiparallel diode) |
| i | Time dependant value of current |
| \hat{i} | Peak value of current |
| $I_{C,NOM}$ | Nominal collector current |
| IGBT | Insulated Gate Bipolar Transistor |
| I_{peak} | Peak value of current |
| I_{ref} | Reference current value of the switching loss measurement |
| I_{RMS} | AC terminal current |
| φ | Conduction angle |
| K_I | Exponent for the current dependency of switching losses |
| K_V | Exponent for the voltage dependency of switching losses |
| L_S | Parasitic inductance / stray inductance |
| M | Modulation index |
| N | Neutral potential (terminal) of a direct voltage source; midpoint between DC+ and DC- |
| NPC | Neutral Point Clamped |
| NTC | Temperature sensor with negative temperature coefficient |

| | |
|-------------|---|
| P | Active power |
| P_{cond} | Conduction power losses |
| P_{SW} | Switching power losses |
| PTC | Temperature sensor with positive temperature coefficient |
| Q | Reactive power |
| r_{CE} | On-state slope resistance (IGBT) |
| r_f | On-state slope resistance (diode) |
| RMS | Root Mean Square |
| R_{th} | Thermal resistance |
| S | Apparent power |
| t | Time |
| THD | Total Harmonic Distortion |
| T_j | Junction temperature |
| TNPC | T-type Neutral Point Clamped |
| TVS | Transient voltage suppressor diode |
| V | Voltage |
| V_{CC} | Collector-emitter supply voltage |
| V_{CE} | Collector-emitter voltage |
| V_{ce0} | Forward threshold voltage (IGBT) |
| V_{f0} | Collector-emitter threshold voltage (diode) |
| V_{CEsat} | Collector-emitter saturation voltage |
| V_{DC} | Total supply voltage (DC+ to DC-) |
| V_{ref} | Reference voltage value of the switching loss measurement |
| V_{RMS} | AC terminal voltage |

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