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Thyristor Triggering and Protection of Diodes and Thyristors

1. General

Mains (line frequency) thyristors and diodes are used in large numbers in line-commutated converters due to their robustness, low forward losses and comparatively low cost. This application note is limited to the most important applications of mains diodes and thyristors such as bridge rectifiers and AC controllers. The first section concerns relevant parameters for turning on thyristors as well as the demands on the trigger pulse generator and possible topologies. The second part of this application note deals with the selection according to the reverse voltage of mains diodes and thyristors as well as protective measures against internal and external overvoltages. Finally, the possibilities for overcurrent protection are briefly summarised, excluding the selection of fuses and circuit breakers. Please refer to [2] for a detailed explanation of fuse function, characteristic definitions, and selection according to current load and cooling.

2. Requirements to Trigger Mains Thyristors

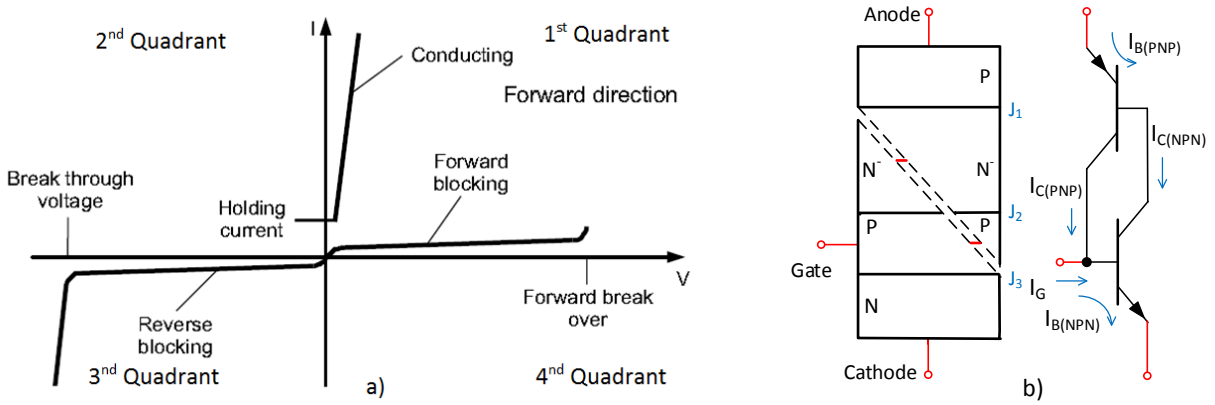
2.1 Trigger process

In the first operating quadrant of the characteristic field (Figure 1a), thyristors can be switched from the forward blocking state to the on state by means of a trigger signal.

In the two-transistor equivalent circuit of a thyristor (Figure 1b), a positive trigger current I_G can flow in the forward direction through the gate-cathode PN junction, J_3, and affect an injection of electrons from the N-cathode (emitter of the NPN transistor). These electrons amplify I_G, and via J_2 in part reach the low-doped N^- zone, represented by the collector of the NPN and base of the PNP transistor. The current in the PNP transistor is amplified by holes injected from the anode (emitter of the PNP transistor) into J_1 and flows through J_2 into the base of the NPN transistor.

The current gains of both transistors increase with current. As soon as the sum of the gate and anode currents is high enough that the sum of the current gains becomes $\alpha_{NPN} + \alpha_{PNP} \geq 1$, the thyristor "fires" and the characteristic curve changes from the "Forward blocking" to "Conducting" state. If the forward current reaches the latching current, I_L, the thyristor remains in the on state even if the trigger current is removed. If later the forward current drops below the holding current I_H, the thyristor returns to the forward blocking state.

Figure 1: a) Current-voltage characteristics and operating areas of symmetrical thyristors, b) two-transistor equivalent circuit diagram

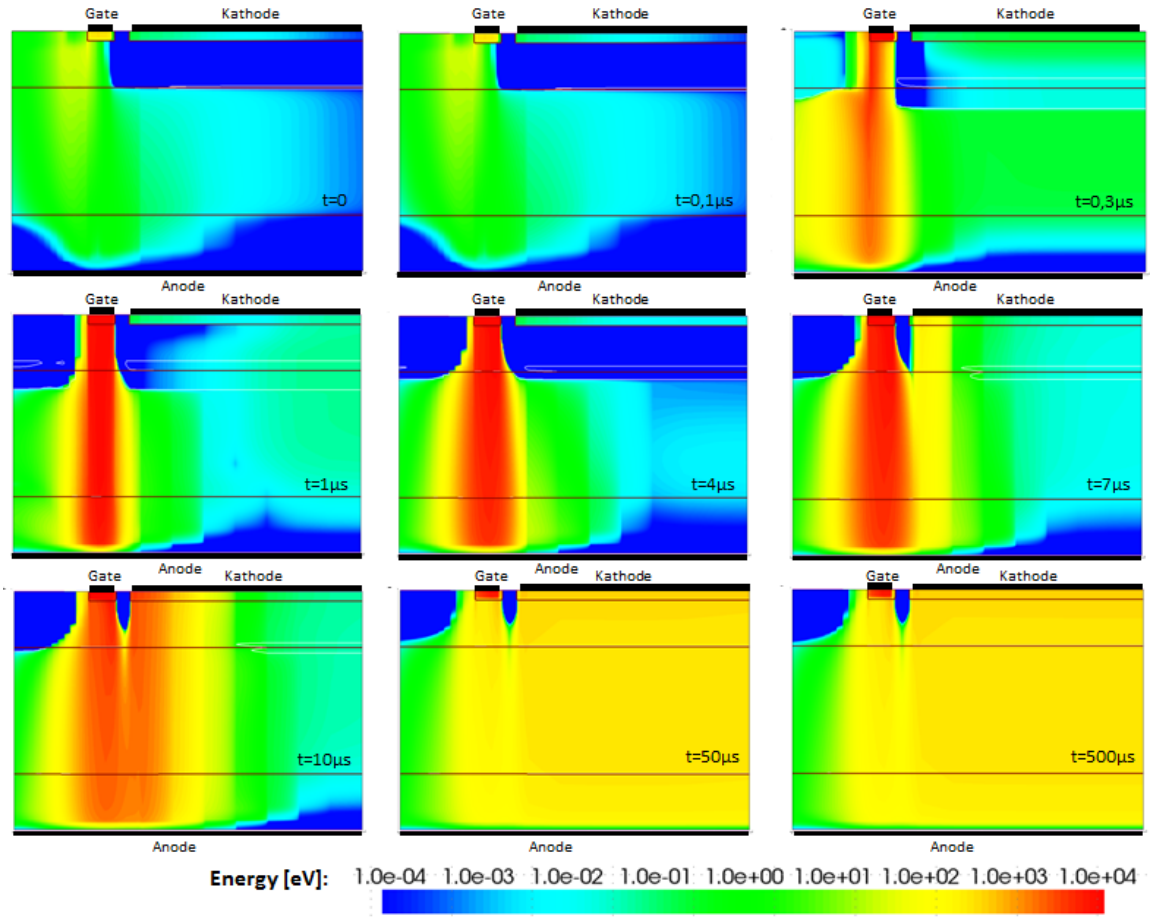


2.2 Dynamic sequence of the trigger process

The trigger process starts locally at the boundaries of the gate, as this is the area of the highest trigger current density. In mains thyristors the propagation of the triggered area is relatively slow with a speed of about 30 - 100µm/µs. This low propagation speed initially leads to very high current densities and intense local heating of the gate, depending on the load current slope which is limited by the external circuitry. In fast thyristors designed for use in self-commutating circuits, the trigger process is faster. However, due to higher conduction and blocking losses as well as a more expensive production cost, these are used only with line-commutated circuits in special cases.

Figure 2 shows the simulation results of the time-dependent current density distribution within 500µs after switching-on the gate current when triggering a 500A mains thyristor. The colors of the areas represent the local loss-energies, which are proportional to the current density. At the beginning of the trigger process, the current density initially increase sharply under the gate area and reaches its maximum between 1µs and 4µs (third and fourth image). Starting on the fifth image the ignition front starts spreading over the entire chip area. After about 50µs (eighth image) in this model the entire thyristor is triggered. At this time, the current density is almost uniformly distributed over the surface.

Figure 2: Simulated loss energy distribution inside a thyristor chip during triggering a I_T of 500A



The finite speed of propagation of the trigger front and the available dissipation of losses results in the limit value "*critical rate of rise of on-state current* $(di/dt)_{cr}$" given in the data sheets as discussed in detail below.

2.3 Impermissible triggering

Triggering conventional thyristors by means other than supplying current to the gate is not permitted, as this is not a defined control pattern. Impermissible triggering may be caused by any current that flows via J_3 from the gate zone to the cathode zone, due to, for example:

- parasitic current from the drive circuit (glitches, inductive or capacitive interference on the control lines, etc.)
- blocking current generated thermally and/or by a high forward blocking voltage leading to breakover triggering when exceeding the zero-threshold-voltage
- very high intensity light or radiation
- capacitive displacement current caused by steeply rising forward-off-state voltage.

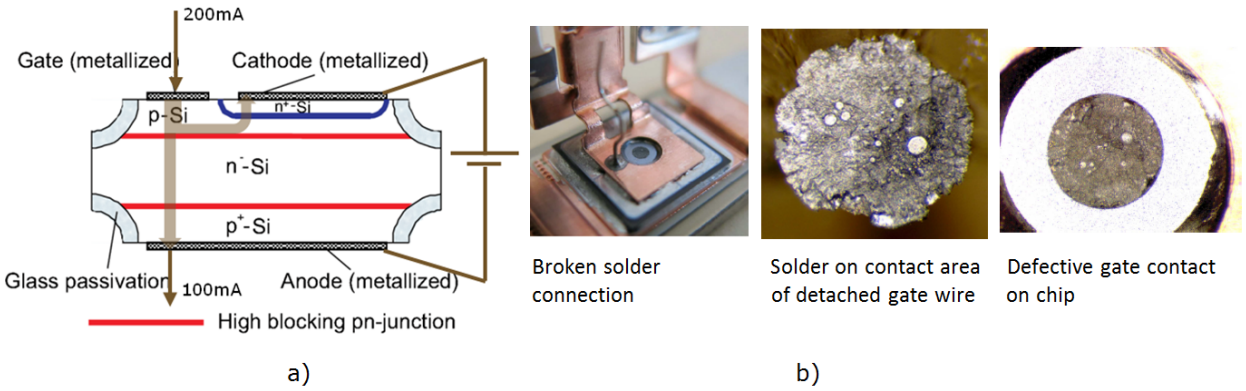
This leads to an inter-dependency of some trigger conditions (e.g. amplitude, rate of rise and duration of gate current) and conditions in the load circuit.

The limit of impermissible triggering of a thyristor due to the steeply increasing off-state voltage is the *critical rate of rise of (forward) off-state voltage* $(dv/dt)_{cr}$, listed in the data sheets. The test condition for SEMIKRON thyristors is an exponential voltage rise up to 66% of the repetitive peak off-state voltage V_{DRM} at the maximum junction temperature T_{vjmax} and an open gate. At lower T_{vj} or lower off-state voltages, $(dv/dt)_{cr}$ is slightly higher. A RC parallel circuit for limiting internal overvoltages (see section 4.2.2) in combination with a suitable line inductance also limits dv/dt.

The final destructive failure mode resulting from impermissible triggering is a $di/dt_{(crit)}$ failure.

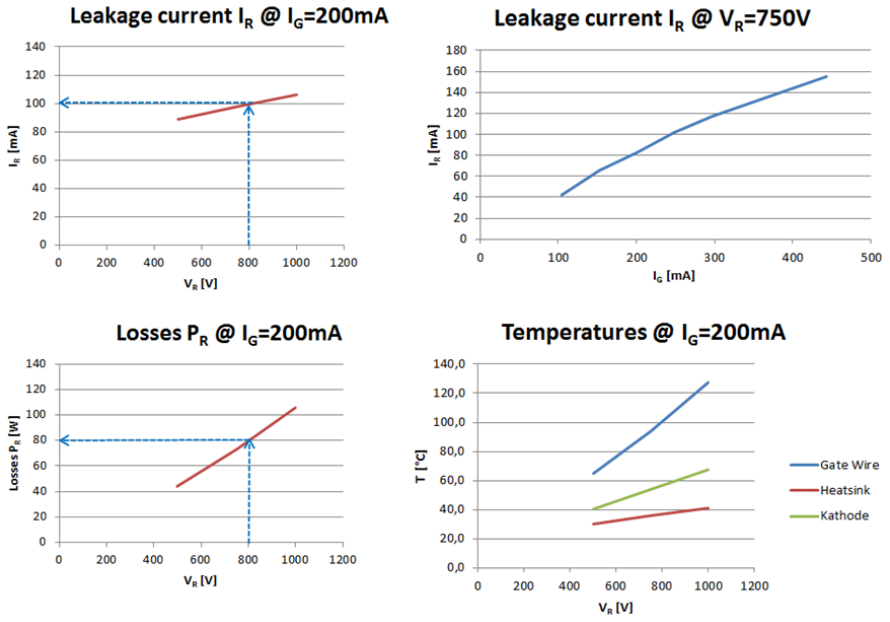
Danger of destruction also exists with incomplete trigger if "regular" trigger pulses are insufficient for complete trigger or, if during the reverse blocking phase (3rd quadrant in the characteristic field), trigger pulses are generated and current is injected into the gate. The trigger current then causes a strong increase in reverse current i_R and thus of the blocking losses in the thyristor (Figure 3a).

Figure 3: a) Sectional drawing of thyristor with current flow from gate to cathode and anode (brown), b) Failure pattern of a thyristor chip inside a SEMIPACK 1 module



As the measurements in Figure 4 show, a gate current of 200mA is amplified in the inversely operated NPN transistor with a current gain of 0.5. Simulations show that at a reverse blocking voltage of V_R = 800V this causes a reverse current of $I_R \approx$ 100mA, i.e. about 80W local losses within the N^-/P^+ - depletion layer under the gate contact. In a 100A thyristor, these losses occur within an area of about 2mm² and heat the silicon locally to temperatures >200°C due to the high thermal resistance caused by the small area. Because of cyclic overheating, the thyristor may fail at the gate contact (Figure 3b).

Figure 4: Measured values of leakage current I_R at reverse voltage V_R = 800V and gate current I_G = 200mA in a 1600V / 50A thyristor module



2.4 Parameters for critical rate of rise of on-state current $(di/dt)_{cr}$ and protective measures

The *critical rate of rise of on-state current* $(di/dt)_{cr}$ indicated in thyristor data sheets is the highest permissible increase in forward current without damaging the thyristor. Thyristors with different gate structures (perimeter gate, central gate and amplifying gate) have different permissible values of $(di/dt)_{cr}$.

Table 1 qualitatively illustrates the dependence of the thyristor (di/dt)–capability on some circuit parameters and operating conditions. This means that, for example, the (di/dt)–capability decreases as T_{vj} or V_D increases. The (di/dt)–capability also increases with increasing I_G, di_G/dt, or trigger pulse duration t_p.

Table 1: Dependence of the (di/dt)-capability on chip temperature T_{vj}, operating voltage V_D, forward current I_T, mains frequency f, amplitude I_G, slew rate di_G/dt, and pulse duration t_p of the trigger current.

	T_{vj}	V_D	I_T	f	I_G	di_G/dt	t_p
(di/dt)–capability	↘	↘	↘	↘	↗	↗	↗

The SEMIKRON data sheet values for $(di/dt)_{cr}$ apply for a frequency of 50/60Hz, a current amplitude I_T of three times the mean forward current $I_{T(AV)}$ of the thyristor at sinusoidal half-wave, a case temperature of 85°C and gate current pulses $I_G = 5 \cdot I_{GT}$ with di_G/dt greater or equal to 1A/µs and gate trigger pulse duration ≥ 10µs.

Despite large inductances in the mains supply, steep current slew rates are possible at turn-on of a thyristor, e.g. due to commutation with capacitances within the converter. In such cases, a limitation of di_T/dt is required using a series inductance L_R (Figure 5):

$$L_R \geq \frac{V_D}{(di/dt)_{cr}}$$

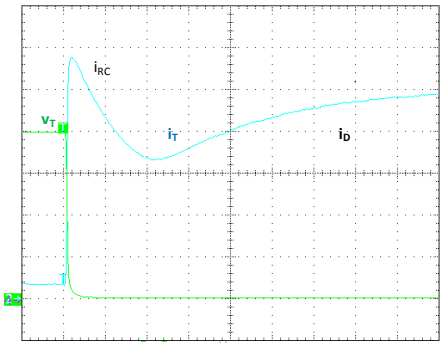
$$L_R \geq \sqrt{2} \cdot \frac{V_V}{(di/dt)_{cr}}$$

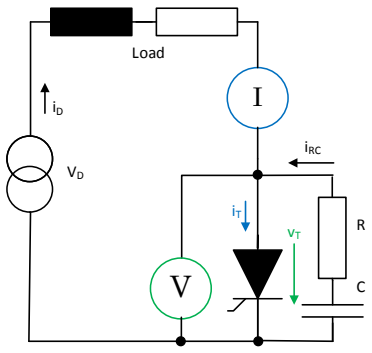
V_V: RMS supply voltage (Line-Line)

A linear inductor in series reduces the current density in the triggered area during the current rise. If a saturating choke is used, the high current slew rate occurs only after the step time t_{St} once a larger area of the thyristor is involved in the current conduction.

A low inductance snubber parallel to the thyristor (see section 4.2.2) causes an additional di_T/dt load when switching onto a high voltage instantaneous value due to the discharged capacitor current (Figure 5). For SEMIKRON thyristors, the peak value of this discharge current must not exceed 50A.

Figure 5: Discharge current of a snubber circuit parallel to the thyristor when switching on and test circuit





2.5 Thyristor control characteristics

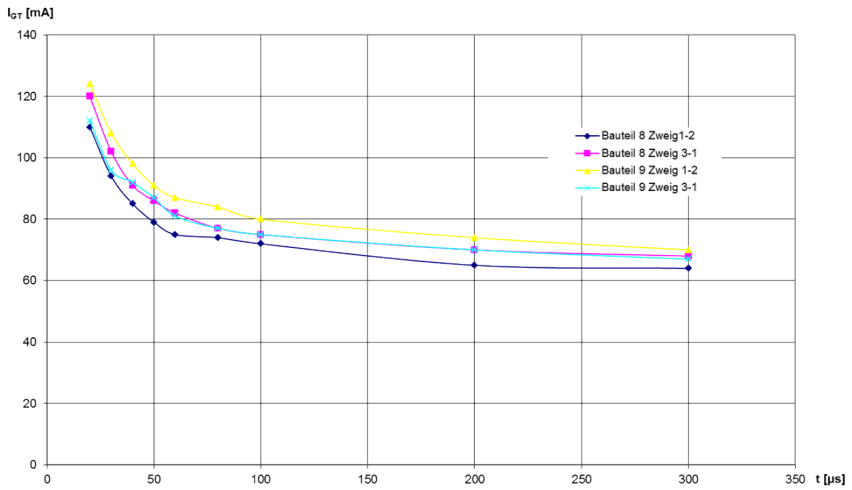
Table 2 shows a section of the data sheet of a SEMIPACK thyristor module SKKT 106 with the data relevant for the design of the trigger circuit. For the data sheet measurements, the thyristors are triggered with DC pulses. In practical applications, DC control must always take into account the gate power losses, which must remain below the limits shown in Figure 7.

Table 2: Data sheet details for design of the trigger circuit (black) and explanations (blue)					
Symbol	**Characteristics**	**Conditions**	**Values**	**Units**	**Specified @**
I_H	Holding Current	T_{vj} = 25°C;	150/250 typ. / max.	mA	V_D = 6V, R-Load
I_L	Latching Current	T_{vj} = 25°C; R_G = 33Ω;	300/600 typ. / max.	mA	V_D = 6V, R-Load; 10µs rect. gate pulse with 5·I_{GT}, R_G = 33Ω
V_{GT}	Gate trigger voltage	T_{vj} = 25°C; d.c.	min. 3	V	V_D = 6V, R-Load; 100µs rect. gate pulse with 5·I_{GT}, R_G = 33Ω
I_{GT}	Gate trigger current		min. 150	mA	
V_{GD}	Highest gate non-trigger voltage	T_{vj} = 130°C; d.c.	max. 0.25	V	
I_{GD}	Highest gate non-trigger current		max. 6	mA	

The *latching current* I_L is the lowest anode current at which the thyristor remains in the on state at the end of the trigger pulse and does not turn off at the end of the trigger pulse. Turn-off occurs when the anode current falls below the *holding current* I_H.

Gate trigger voltage V_{GT} and Gate *trigger current* I_{GT} are the minimum values of control current and control voltage, which are required at 100µs pulse width for a guaranteed trigger. Shorter control pulses increase I_{GT} between 1.4- and 2-fold; see the example in Figure 6.

Figure 6: Measured dependency of the trigger current I_{GT} on the trigger pulse width t_p at a 250A SEMIPACK thyristor module



Below the *highest gate non-trigger current* I_{GD} or the *highest gate non-trigger voltage* V_{GD} at the gate, the device will not trigger. Above $V_D \approx 100V$, I_{GD} decreases by up to 30% with increasing voltage.

Table 3 illustrates the dependency of these characteristics on circuit parameters and operating conditions. For example, I_H decreases as T_{Vj} or V_D increases and I_{GT} decreases with increasing T_{Vj}, I_G and di_G/dt.

Table 3: Dependency of trigger parameters I_H, I_L, V_{GT}, I_{GT}, V_{GD} and I_{GD} on chip temperature T_{vj}, operating voltage V_D, amplitude I_G, rate of rise di_G/dt and pulse duration t_p of the trigger current.

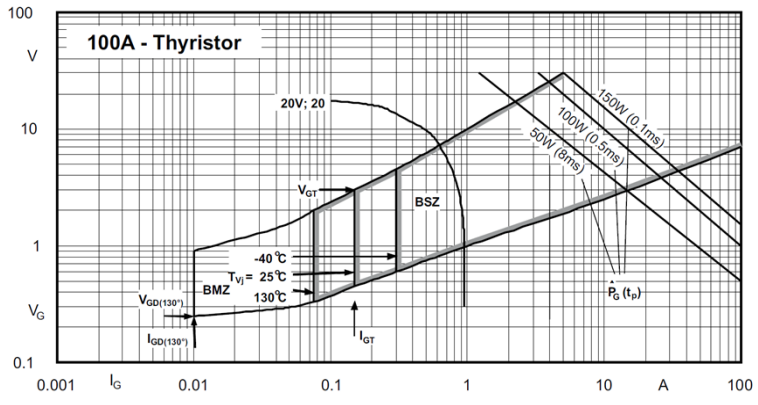
	T_{vj}	V_D	I_G	$di_{G/dt}$	t_p
I_H	↘	↘	-	-	-
I_L	↘	↘	↘	↘	↘
V_{GT}	↘	↗	↗	-	-
I_{GT}	↘	-	↘	↘	↘
V_{GD}	↘	-	-	-	-
I_{GD}	↘	↘	-	-	-

The data sheet mentions values for *gate controlled delay time* t_{gd} and *gate controlled rise time* t_{gr}. These are the time intervals from applying the trigger current until the beginning of the forward voltage decay V_D across the thyristor (t_{gd}) or from the beginning to the end of this decay (t_{gr}) respectively, see also [2], section 3.2.5. The total *gate trigger time* $t_{gt} = t_{gd} + t_{gr}$ depends on the thyristor type and is typically between 3µs and 6µs.

The *gate trigger characteristics* shown in the SEMIKRON data sheets describe the possible deviation ranges of the gate-cathode diode characteristics $V_G = f(I_G)$, see Figure 7. Figure 7 also includes the temperature-dependent trigger ranges and the curves of the maximum trigger power losses P_{GM} for different trigger pulse durations. SEMIKRON's and most other manufacturers' data sheets do not contain a value for the maximum continuous gate power losses for DC operation. Here, P_G should be less than 10W.

Trigger current I_{GT} and trigger voltage V_{GT} at T_{vj} = 25°C as well as highest non-triggering gate current I_{GD} and highest non-triggering gate voltage V_{GD} are marked in the diagram at the maximum permissible chip temperature T_{vjmax} for this thyristor. The *area of possible trigger (BMZ)* and *area of safe trigger (BSZ)* for T_{vj} = -40°C, 25°C and T_{vjmax} are also marked. The I_{GT} sinking with rising temperature causes the BSZ to expand to smaller gate currents as the temperature increases.

Figure 7: Gate-cathode voltage V_G as a function of the gate current I_G (deviation range) with the areas of possible trigger (BMZ) and safe trigger (BSZ) at different chip temperatures T_{vj}, limits of the permissible trigger power loss $P_G(t_p)$ and exemplary characteristics of a trigger circuit (20V; 20Ω)



The current-voltage characteristic of a trigger circuit has to ensure that the current and voltage of the trigger pulses are within the safe trigger range (BSZ) over the full operating temperature range and the *peak trigger power loss* $\hat{P}_G(t_p)$ indicated in the diagram for pulse durations t_p of 100µs, 500µs and 8ms is not exceeded. As an example, the diagram contains the characteristic of a trigger circuit with 20V open circuit voltage and 20Ω internal resistance. An operating point in the BMZ must be avoided for intentional trigger currents as well as residual currents or coupled interference currents that could inadvertently lead to triggering.

2.6 Requirements for the trigger pulses

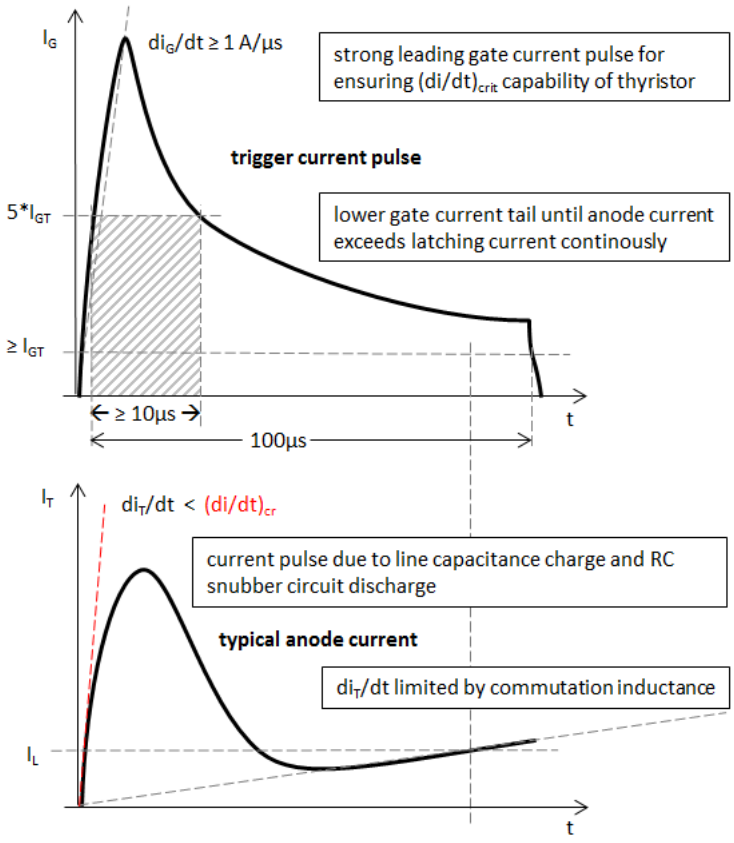
Although a 10µs-long gate current pulse is sufficient to trigger a thyristor under laboratory conditions and with resistive load, the real requirements in practice can be significantly higher.

The shape, amplitude and duration of the trigger pulse must be adapted to:

- the specific control characteristics of the thyristor (control characteristics or data sheet values for V_{GD}, V_{GT}, I_{GD}, I_{GT}, P_{GM} (t_p), t_{gd}, t_r)
- the operating temperature range, since I_{GT} increases at low temperatures
- the progress of the load current (reaching I_L, possible current drop below I_H).

The $(di/dt)_{cr}$ and trigger characteristics - given in the SEMIKRON data sheets and discussed in sections 2.4 and 2.5 above - are validated with trigger pulses according to Figure 8. Shorter trigger pulses have the effects shown in Figure 6 or Table 3 on other parameters.

Figure 8: Recommended trigger current, used to validate SEMIKRON thyristors and general course of the load current with inductive load and snubber wiring

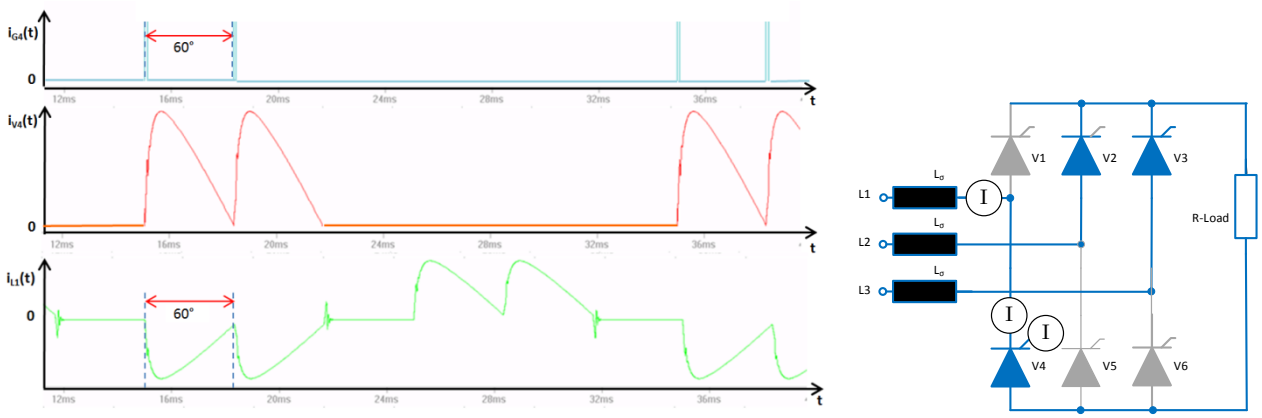


As it is expensive in practice to produce high and long trigger pulses, compromise solutions are often used. In general, the trigger pulse should be at least high ($\approx 5 \cdot I_{GT}$) or long ($\geq$ 20µs), but in any case show a steep increase ($\geq$ 1A/µs) and last at least until reaching I_L. Longer and higher trigger pulses reduce I_{GT} and I_L and increase the thyristor (di/dt)-capability.

For rectifiers with reversing voltage and AC controllers with inductive load, each thyristor cannot fire until the instantaneous value of the supply voltage is higher than that of the reverse voltage. In order to achieve safe commutation, trigger pulses of up to 10ms are required anyway at 50Hz.

In fully controlled six-pulse bridge rectifiers (B6C) and in the case of continuous current flow the thyristors have current conduction angles of 120°. In the case of discontinuous current or indirect commutation via a freewheeling diode, each current block is divided into two blocks with a 60° current conduction angle. The trigger circuit must therefore deliver double pulses with a distance of 60°. Figure 9 illustrates this with simulated currents in phase L1 and thyristor V4.

Figure 9: Current curves in a fully controlled B6 bridge rectifier with discontinuous output current (example simulation for V4)



3. Trigger Circuits

The trigger circuit has to generate current pulses meeting the requirements of section 2 under all operating conditions. This includes the necessity of being synchronised to the mains in order to exclude trigger pulses during the 3rd quadrant reverse blocking state, explained in section 2.3. The pulses that must be blocked can be recognized, for example, by comparing the control signal with the polarity of anode-cathode voltage of each thyristor.

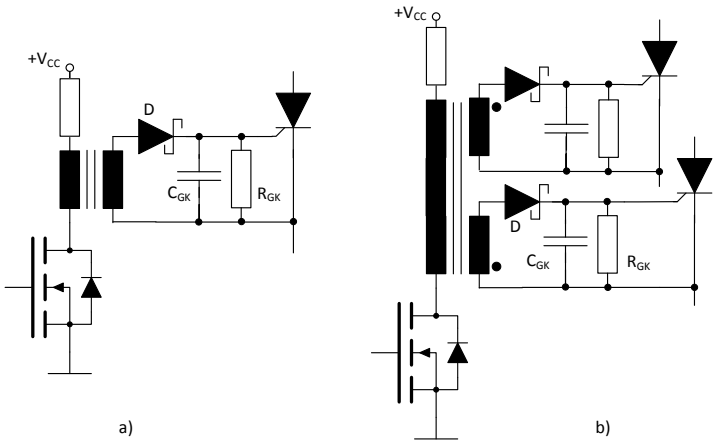
Since the thyristors of a power converter are usually at different potentials, the outputs of the trigger circuits must then be isolated from each other. Pulse transformers are most frequently used for this purpose. These can transmit both the trigger signal and the required control power. Opto-couplers are also used; however, the control power at cathode potential of the thyristor must be generated by a separate power supply or recovered from the anode voltage.

Current and voltage transients can influence the function of the trigger circuit by inductive or capacitive interference or act directly on the control lines of the thyristor and cause unwanted switching. Typical countermeasures are short and twisted control lines, a resistance R_x in the range of about 22 - 220Ω between gate and cathode, and shields between the primary and secondary side in the pulse transformer (or opto-couplers) connected to ground to conduct the current via their coupling capacitance.

3.1 Trigger circuits with pulse transformers

Figure 10 shows conceptual schematics of trigger circuits with pulse transformer.

Figure 10: Conceptual schematics of trigger circuits with pulse transformer: a) triggering one thyristor, b) triggering two thyristors of a rectifier phase



The primary voltage V_{CC} and the winding ratio of the transformer must be selected so that the secondary voltage is high enough to supply a sufficient gate current for the thyristor also at dynamical V_{GK} overshot and with negative feedback during the commutating anode current (see chapters 2.2.2.4 and 3.2.5.2 in [2]).

The fast diode D in the secondary circuit prevents negative gate current during the commutation swing of the transformer secondary voltage and during dynamical V_{GK} overshot. Purpose of the RC-element, R_{GK}, C_{GK} is to filter unwanted glitches on the trigger line. A capacitance, C_{GK} of 10 - 47nF is recommended to achieve a discharge time constant $\tau = R_{GK} \cdot C_{GK} \approx 10$ - 20µs (and $R_{GK} \approx 220$ - 2200Ω). The power loss P_R of R_{GK} at maximum control angle via a half period of line frequency will be:

$$P_R = \frac{V_{GK}^2}{2 \cdot R_{GK}}$$

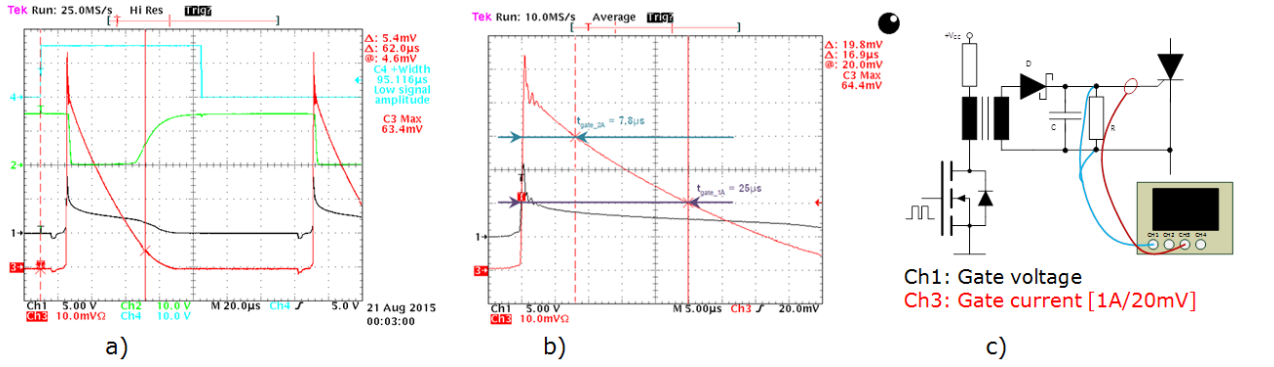
That means at V_{GK} = 5V and extreme values (max. C_{GK} = 47nF, min. R_{GK} = 220Ω) and T ≈ 10µs, P_R is about 60mW. At τ ≈ 22µs with C_{GK} = 10nF and R_{GK} = 2200Ω, P_R would be only about 6mW. The amount of loss $P_{R'}$ resulting from the discharge of C_{GK}:

$$P_{R'} = \frac{C_{GK}}{4} \cdot V_{GK}^2 \cdot \frac{1}{T_{rep}}$$

only comes into play with thyristor control with "Pulse Train" (see Fig. 12). At V_{GK} = 5V, C_{GK} = 47nF and T_{rep} = 20µs this part would be about 150mW, with C_{GK} = 10nF only about 31mW.

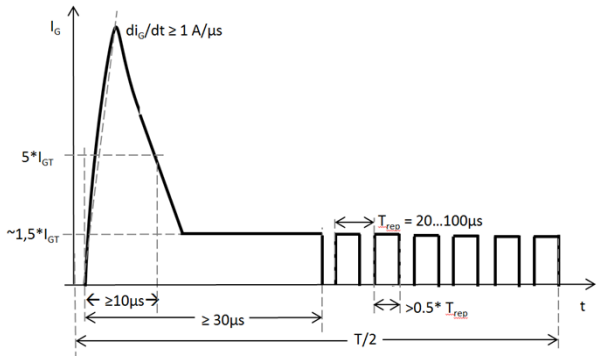
The drive of the pulse transformer can be in either direction, acting as a forward converter or a flyback converter. Figure 11 shows a flyback converter with trigger pulse curves measured with a thyristor connected. If the primary current has stored enough energy in the transformer when the transistor is switched on, the transistor is then switched off for a defined time. The stored energy now drives the secondary current as trigger current through the gate-cathode path of the thyristor. Primary voltage and transformer stray inductances determine the exponential increase of the secondary current.

Figure 11: Gate current and gate-cathode voltage ([3]): a) time resolution 20µs/div, b) time resolution 5µs/div, c) measuring circuitry



In order to trigger thyristors with small and economic trigger transformers using pulse lengths of a few milliseconds, oftentimes a "pulse train" or "picket fence" triggering as shown in Figure 12 is used, consisting of a 10µs current peak, a short constant current phase and 5 - 40kHz square wave pulses for the rest of the duty cycle. If a flyback converter is used, these pulses can easily be controlled by means of current control. It is also possible to use a monostable multivibrator or a microcontroller to generate the trigger pulse sequence.

Figure 12: Gate trigger current for a "pulse train"



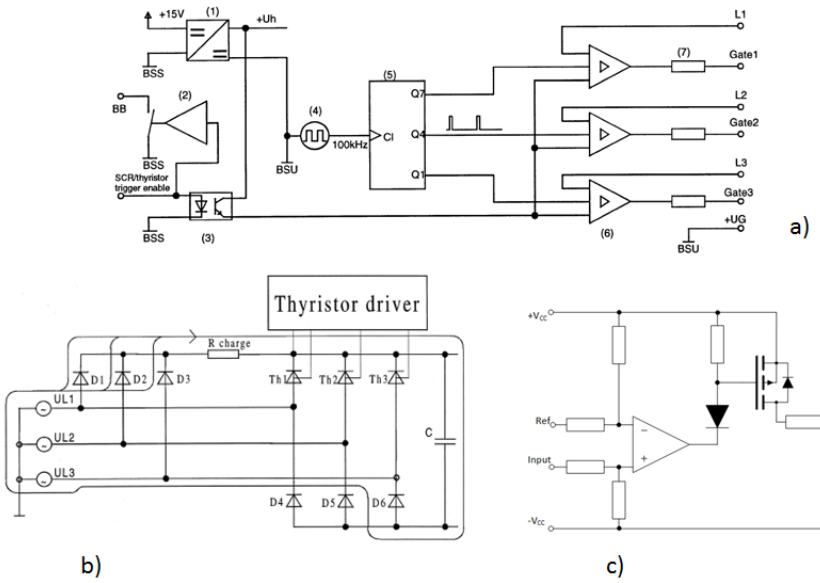
Details on the function and selection of trigger transformers are described in [2], section 4.3. In the data sheets of a trigger transformer, these are characterised by the following parameters ([4], [5]):

- *Number of windings* primary to secondary and transmission ratio between the windings (1:1, 2:1, 2:1:1)
- *Trigger current* I_{ign}: primary current peak value, at which the voltage drop across the winding resistance is still insignificant, e.g. < 1V
- *Rated voltage* V_{nom}: secondary-side RMS voltage for which all insulation distances are dimensioned, i.e. 380V, 500V, 750V, 1kV
- *Test voltage* V_p: Insulation test voltage according to V_{nom}
- *Voltage-time integral* V_0t: The voltage induced in the secondary winding $V_0 = -L_\sigma \cdot di_p/dt$ decreases after the current increase of a square wave pulse on the primary side during the time t_p, which is inversely proportional to the voltage V_0. Since on the secondary side the voltage amplitude of the pulse is determined by the gate characteristic and by the series resistances in the circuit, V_0t of a trigger transformer defines the width of a single trigger pulse. (Minimum value at the secondary winding at no load until saturation). Typical values are between 180Vµs and 5kVµs.
- *Rise time* t_r: rise time of the secondary current at a defined load resistance R_L i.e. (depending on manufacturer) for 10…90% of the maximum value I_M. The rise time t_r is proportional to the time constant of stray inductance L_{sp} + L_{ss} and load resistance R (sum of all resistances in the gate circuit).
- *Primary inductance* L_p: measured at 1kHz and open secondary, dependent on the number of turns and permeability of the core material.
- *Stray inductance* $L_s = L_{sp} + L_{ss}$: measured at a secondary winding at 10kHz and shorted primary winding; depends on the number of turns and the design of the transformer.
- *Winding resistances* R_p (primary winding) and R_s (secondary winding)
- *Coupling capacitance* C_{ps} between primary and secondary winding: can cause unwanted trigger of the thyristor by voltage jumps of the thyristor potential (secondary side) due to the miller effect. Existing shield windings between the primary and secondary windings therefore are to be connected to ground.

3.2 Trigger circuits with opto-couplers

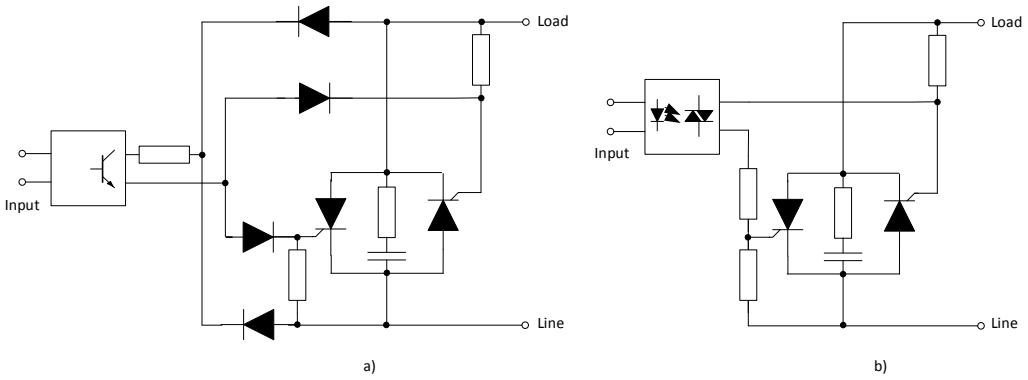
Opto-couplers can also be used to isolate the potential of trigger signals. Since the required trigger power cannot be transmitted, a separate secondary voltage supply at cathode potential is necessary in each case. A frequent example of application is a rectifier bridge with several thyristors connected at the cathode side, i.e. half-controlled six-pulse bridges (B6HK), as they are often used for DC link pre-charge. For this topology, SEMIKRON offers the thyristor driver SKHIT 01 [6], which keeps the thyristors blocked via the diodes D1-D3 during the pre-charging of the DC-bus capacitors (Figure 13). After the charging process, the SKHIT 01 permanently triggers the thyristors while they are in forward direction, while supressing trigger signals when the thyristors are reverse biased.

Figure 13: DC link pre-charging via B6HK bridge with control by SKHIT 01 and trigger circuit of a thyristor: a) Block diagram, b) Main circuit diagram, b) Trigger unit for one thyristor



What are not recommended by SEMIKRON are very simple solutions for obtaining the trigger power from the operating voltage. Here undefined transient conditions can occur during the operation of such circuits. Such circuits are shown in Figure 14 and sometimes suggested for simple applications like AC-controllers with zero-crossing control. In Figure 14a, the trigger signal is controlled by an unipolar switch ([7]). Figure 14b shows a further simplification of this circuit by using an opto-triac for potential separation which can switch in both directions; e.g. the IL421x from Vishay ([8]).

Figure 14: Not recommended thyristor controls from the anode voltage: a) SCR SSR circuit [7], b) simplified circuit with opto-triac



4. Off-State Voltages and Overvoltage Protection

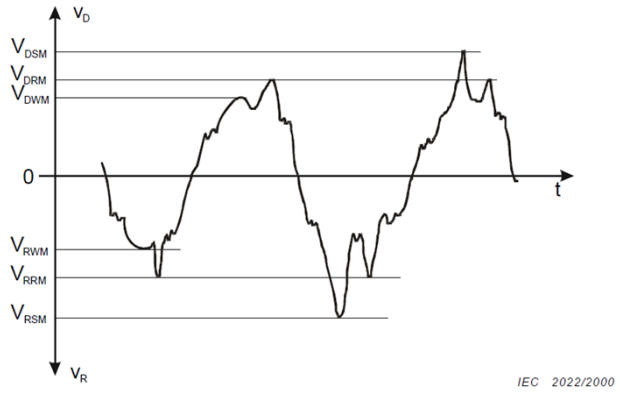
When selecting diodes and thyristors, it must be taken into account that the voltage limit values V_{DRM}, V_{RRM}, V_{DSM} and V_{RSM} listed in the data sheets are defined as peak values of sine half-waves. These values are specified for an open (not connected) gate terminal. For constant DC load, manufacturers recommend for the maximum values $V_{D(DC)}$ (thyristors) or $V_{R(DC)}$ (thyristors and diodes) not to exceed 50% of V_{DRM} or V_{RRM}.

Overvoltage protection for power semiconductors in line-commutated converters may be necessary to protect from "internal" and "external" overvoltages, depending on the cause of the overvoltage, on the AC side, DC side, or parallel to the thyristors/diodes respectively.

4.1 Selection of diodes and thyristors according to the repetitive peak reverse voltage

Even with the highest possible voltage stress (upper mains voltage tolerance limit plus overvoltages), the maximum permissible reverse voltages V_{RSM}, V_{RRM}, V_{DSM} and V_{DRM}) according to Figure 15 must not be exceeded; see definitions according to IEC 60747-6, see [9] and [2], sections 3.2.4.1 and 3.2.5.1.

Figure 15: Example of a line voltage characteristic with crest (peak) working off-state voltage V_{RWM}, repetitive peak off-state voltage V_{RRM} and non-repetitive peak off-state voltage V_{RSM} ([9])



For use at very low temperatures, it must be considered that the blocking voltages given in some data sheets are specified for temperature ranging from 25°C to T_{vjmax}. Due to the positive temperature coefficient of the breakdown voltage, this decreases with T_{vj} by about 0.11%/K. In contrast the reverse currents decrease with temperature T_{vj} by about $0.96^{(Tvjmax-Tvj)}$, as well as does the risk of unintended trigger.

Expected overvoltages and sensible overvoltage protection measures determine not only the projected service life of the device (e.g. FIT-rate as a function of cosmic radiation), but also the voltage headroom required for semiconductor selection.

In order to withstand operational overvoltages, thyristors and diodes are operated at supply voltages V_V, of which the peak value is not higher than the peak reverse voltage divided by a safety factor k. For industrial applications on low-voltage mains supply, k should be selected in the range of 1.5 - 2.5.

$$\sqrt{2} \cdot V_V = V_{DWM} = \frac{V_{DRM}}{k} \quad resp. \quad \frac{V_{RRM}}{k}$$

A low safety factor is applied when the expected voltage stress is basically known, for example when the rectifiers are connected to DC-bus with little inductance. For converters in low-voltage supply networks with unknown overvoltages, safety factors of 2 - 2.5 are recommended, depending on the available blocking voltage classes of the diodes and thyristors, see Table 4.

Table 4: Recommended blocking voltages for thyristors and rectifier diodes depending on the rated voltage of the supply

Line Input Voltage V_V [V]	Rectifier Connection	Direct Output Voltage V_{di0} [V]	Peak Voltage $\sqrt{2} * V_V$ [V]	Recommended Blocking Voltages V_{DRM}, V_{RRM} [V]	Safety factor k
125	Line-Neutral	110	177	600	3.39
230	Line-Neutral	202	325	800	2.46
400	Line-Line	540	566	1400	2.47
480	Line-Line	648	679	1600	2.36
500	Line-Line	675	707	1800	2.54
575	Line-Line	776	813	2000	2.46
600	Line-Line	810	848	2000	2,36
660	Line-Line	891	933	2200	2.36
690	Line-Line	932	976	2200	2.25

Line-Neutral: single-phase circuit
Line-Line: three phase circuit

4.2 Internal overvoltages and protective measures

In contrast to external overvoltages, internal overvoltages are caused by the turn-off behaviour of the diodes or thyristors. Amplitude and shape of the internal overvoltage depend on the impedances of the commutation circuits.

4.2.1 Turn-off behavior of mains diodes and mains thyristors

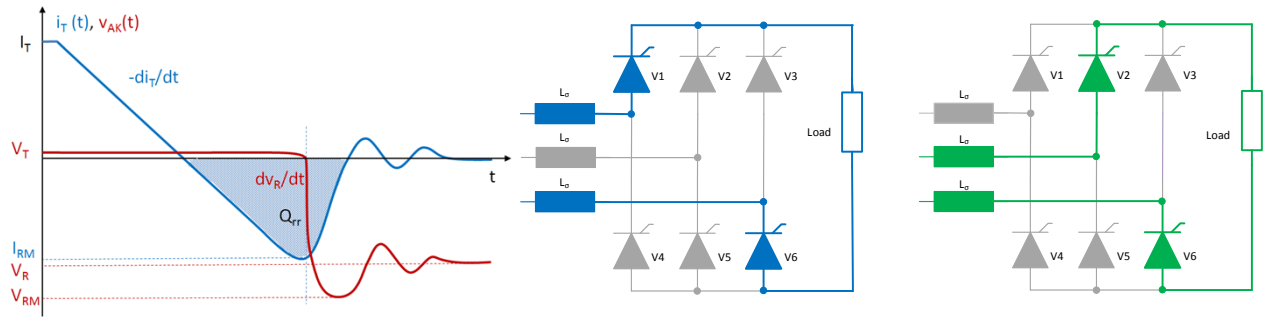
Diodes and thyristors for mains application have a PIN structure that consists of a heavily doped P^+ layer, a heavily doped N^+ layer and a weakly doped N^- layer, also called the I (intrinsic) layer. The doping profile and width of the I-layer determine the maximum blocking voltages. At forward current, the I-layer is flooded by charge carriers. The majority of these charge carriers have to be depleted to be able to pick up voltage in reverse direction when the anode–cathode voltage is reversed. Residual positive charge carriers (holes) still present in the I-layer cause the anode current to not stop at the zero crossing but to continue to flow for a short time in the reverse direction as a reverse recovery current ("HSE: Hole Storage Effect"). After a recovery peak,

$$I_{RM} \tilde{} \sqrt{(0.77 \cdots 1) \cdot I^{-di_T/dtI} \cdot Q_{rr}}$$

decays steeply, which causes a voltage peak $V_{L\sigma} = -\Sigma L_\sigma \cdot di_T/dt$ at the inductances L_σ of the load circuit, which adds to the blocking voltage (Figure 16).

This "internal" overvoltage occurs each time a diode or thyristor is turned off, in addition to "external" overvoltages from the grid or caused by the load.

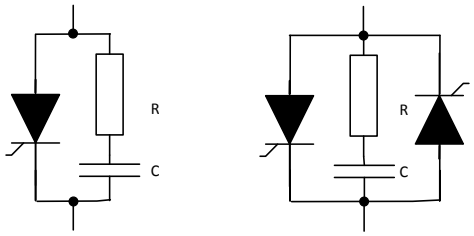
Figure 16: Current and voltage curves during the transition of V1 from the conduction to the blocking state (Commutation from V1/V6 to V2/V6)



4.2.2 Snubber circuits

The most common way to protect thyristors against internal overvoltages and to limit dv/dt is to use "HSE" snubber circuits consisting of RC networks in parallel with the individual thyristors (Figure 17).

Figure 17: Snubber circuits: a) of a single thyristor, b) of an AC controller



The snubber circuits extend the inductors present in the load circuit to form series resonant circuits, transforming voltage spikes into dampened oscillations of low amplitude. The energy of the overvoltage is thus forced to decay not over a short term with high power but with low power over a longer period.

For uncontrolled (diode) bridge rectifiers, it is sufficient in most cases to connect only the DC side with an RC-element or, in the case of diodes with sufficient current rating, with only one capacitor, as this circuit is effective with each commutation.

4.2.3 Dimensioning of snubber circuits for SEMIKRON thyristors

The rating of a snubber circuit depends (among others) on i_{TM} (i_{FM}) before turn-off, the -di$_T$/dt (–di$_F$/dt) of the forward current, the reverse current peak I_{RM}, the peak reverse voltage V_{RM}, in relation to V_{RRM} of the device, and, for thyristors, the critical voltage rise time $(dv/dt)_{cr}$ to be observed.

Table 5 contains the design recommendations for SEMIKRON thyristors and thyristor modules for "common" operating conditions, such as

- safety factor of V_{RRM} for the peak value of the terminal voltage ≥ 2.2
- short-circuit voltage of the converter transformer u_K ≥ 5% or mains choke, in which the inductance L of the choke in each phase is such that a short-circuit voltage of at least 5% of the supply voltage V_V results:

$$L \geq 0.05 \cdot \frac{V_V}{2 \cdot \sqrt{3} \cdot \Pi \cdot f \cdot I_V}$$

V_V: RMS supply voltage (Line-Line)
I_V: RMS phase current
f: grid frequency

Table 5: Recommended snubber circuits for SEMIKRON thyristors

Line Input Voltage V_V [V]	Snubber Data	Mean forward current I_{FAV}, I_{TAV} [A]				
		≤25	≤100	≤250	≤500	>500
≤250	**C [µF]**	0.22	0.22	0.22	0.47	application specific
	R [Ω]	68	33	33	33	
	P_{Rmin} [W]	6	10	10	25	
≤400	**C [µF]**	0.22	0.22	0.22	0.47	
	R [Ω]	68	47	47	33	
	P_{Rmin} [W]	6	10	10	25	
≤500	**C [µF]**	0.1	0.1	0.1	0.22	
	R [Ω]	100	68	68	47	
	P_{Rmin} [W]	10	10	10	25	
≤690	**C [µF]**		0.1	0.1	0.22	
	R [Ω]		100	100	68	
	P_{Rmin} [W]		10	10	50	

P_{Rmin}: Recommended snubber resistor power rating

At very low voltage safety factors or other deviations from the above conditions, the snubber rating may need to be adjusted. Literature details recommendations for simulation-based design, e.g. 0.

Easier options for rough estimates are described in [2], section 4.4.2.1:
Assuming that approximately half of the energy represented by the reverse recovery charge Q_{rr} is transferred to the circuit as overvoltage, approximate values for the capacitance C and the damping resistance R can be determined as follows:

$$C = \frac{Q_{rr}}{\sqrt{2} \cdot V_V}$$

$$R = (1.5 \ldots 2) \cdot \sqrt{\frac{L_s}{C}}$$

C [µF]: Snubber capacitance
V_V [V]: RMS supply voltage (Line-Line)
L_s [µH]: total load circuit inductance
R [Ω]: Snubber resistance
Q_{rr} [µC]: Reverse recovery charge
f [Hz]: Line frequency

As mentioned in section 2.4, for SEMIKRON thyristors, the current amplitude must not exceed 50A when discharging C via R during trigger. It is therefore possible that R must be increased at the expense of overvoltage attenuation.

The power loss P_R [W] in the damping resistor R can be determined by the following equation:

$$P_R = \sqrt{2} \cdot V_V \cdot 10^{-6} \cdot Q_{rr} \cdot f + k_1 \cdot C \cdot V_V^2 \cdot f$$

k1 = 0 for diodes in uncontrolled bridge rectifiers
k1 = $2 \cdot 10^{-6}$ for thyristors in controlled one- and two-pulse centre tapped circuits, and thyristors and diodes in half-controlled two-pulse bridge circuits
k1 = $3 \cdot 10^{-6}$ for thyristors in controlled three- and six-pulse centre tapped circuits as well as fully controlled two-pulse bridge circuits and AC-controllers
k1 = $4 \cdot 10^{-6}$ for thyristors and diodes in fully or half-controlled six-pulse bridge circuits

Further calculations as well as suggestions for modified circuits and circuit combinations are given in [2], section 4.4.2.1 through 4.4.2.3. Since AC-controllers (W1C, W3C, W3C2) consist of two anti-parallel thyristors per phase, both use a common RC-circuit (Figure 17b), which limits internal and external overvoltages. A large commutation dv/dt can occurs here at inductive load and triggering at phase angel α > 0° el. The snubber must limit this below $(dv/dt)_{cr}$ for the still turned off thyristor. Section 4.4.2.2 in [2] contains an approximate method to estimate C [µF] and R [Ω] of the snubber circuit by means of the following equations:

$$C \sim 700 \cdot \frac{I_V}{{V_V}^2}$$

$$R \sim \frac{9000}{C \cdot \mathrm{V_V}}$$

V_V [V]: RMS supply voltage (Line-Neutral)

The power loss P_R [W] of the resistor R is about:

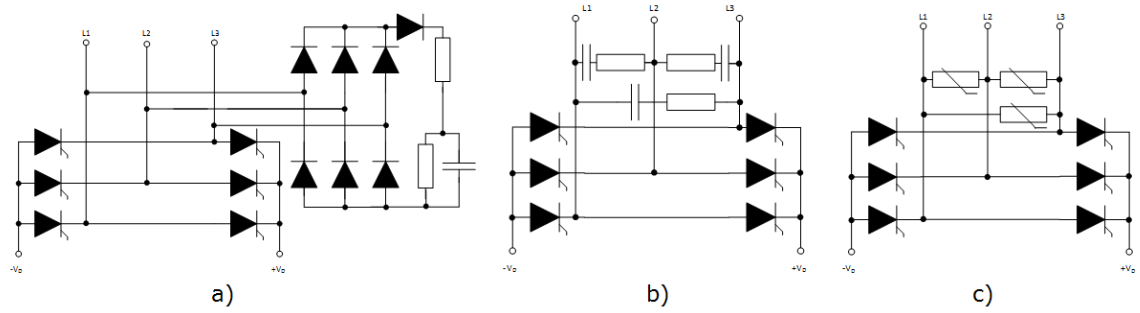
$$P_R \sim 3 \cdot 10^{-6} \cdot \mathrm{C} \cdot \mathrm{V_V^2} \cdot \mathrm{f}$$

4.3 External overvoltages and protective measures

External overvoltages are generated, for example, by switching operations on the grid, the triggering of breakers or lightning strikes. Protective measures are possible on both the AC and DC side.

In the lower current range, the snubber circuitry described above can often be rated so that it also protects sufficiently against external overvoltages. For high power levels, however, additional snubbering on the AC side makes sense, for which Figure 18 shows three options that can also be combined.

Figure 18: AC-side overvoltage protection circuits for bridge rectifiers: a) by auxiliary bridge, b) by RC snubbers, c) by varistors



More detailed information on the function and calculation of AC-side snubber circuits, other snubber options and the use of avalanche diodes and varistors to limit overvoltages are given in [2], sections 4.4.2 through 4.4.4.

5. Overcurrent Protection of Diodes and Thyristors

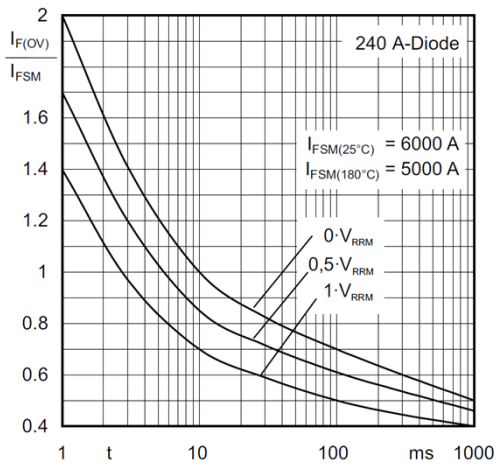
Diodes and thyristors cannot actively limit or switch off overcurrent. A steep increase in chip temperature associated with excessive load current can cause the temporary loss of controllability and blocking capability. Therefore, certain specified overloads are allowed only at intervals of several seconds and only occasionally with a limited number of periods.

In case of a permissible overload the surge current determined by the grid impedance and mains voltage has to be survived. For this reason, data sheets contain a diagram showing the overcurrents $I_{T(OV)}$ or $I_{F(OV)}$ permitted in the event of a fault (short circuit) in relation to the surge current limit value I_{FSM} at different blocking voltages (Figure 19). If a fuse or other protective device responds due to a high current, the curve

for V_{RRM} = 0 applies. If the current is limited by external measures, the current decreases analogously to the other two curves.

The current values above 10ms are valid for sinusoidal current pulses with a pulse time of 10ms, which recur at intervals of 20ms.

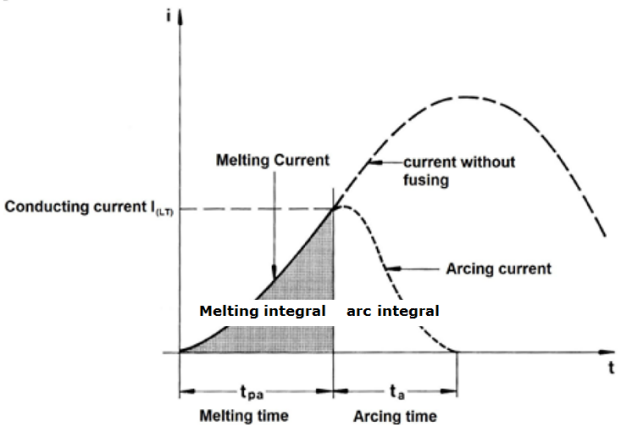
Figure 19: Permissible overcurrents $I_{F(OV)}$ (or $I_{T(OV)}$ for thyristors) in the event of a fault in relation to the surge forward current I_{FSM} at different off-state voltages as a function of the time t



The selection of overcurrent protective devices depends on the expected overcurrent load. Long-term protection should prevent thermal overload due to high current or cooling problems. If a current or temperature sensor indicates that the limit value has been exceeded, (in the case of thyristors) the phase angle is increased or the trigger pulses are blocked. Alternatively, the forward current can be interrupted by circuit breakers or overcurrent devices. The tripping characteristics of the protective devices must be below the overcurrent limit for short-time operation so that the blocking capability of the thyristors or diodes is completely maintained.

A short-term protection limits the overcurrent caused by a short circuit to a value safe for the thyristors or diodes in the time domain up to one half-sine. This can be done with fast semiconductor fuses that melt within a few milliseconds with a characteristic depicted in Figure 20.

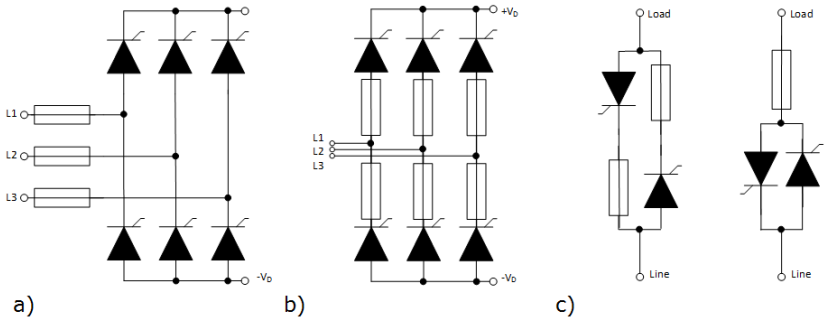
Figure 20: Current profile when switching off a short circuit with a semiconductor fuse



t_{pa}+t_a = turn-off time (~ 3...5ms)

Typical arrangements of semiconductor fuses in power converters are shown in Figure 21.

Figure 21: Arrangements of the semiconductor fuses in bridge converters: a) as branch fuses, b) as line fuses, and in AC-controllers (c)



For cost and space requirements as well as the necessary spare parts stock, fuses today are only used in the upper power range. An alternative are circuit breakers with thermal-magnetic tripping.
In extreme cases, when the fuse or circuit breaker trips, the load integral i^2dt given in the data sheet of the semiconductor can be exploited. Since the response time depends on the level of overcurrent, for high impedances in the short-circuited branch there might not always be sufficient protection possible.

With regard to the selection possible in relation to the effort, it must be decided whether the thyristors or diodes must be "rescued" in the event of overcurrent or only the gravity of defects should be limited. Detailed recommendations on selecting semiconductor fuses are given in [2], section 4.4.6.2.

Symbols and Terms

Letter Symbol	Term
α	Phase angel (triggering thyristors)
C	Capacitor, capacitance
C_{ps}	Coupling capacitance (pulse transformer)
C_{GK}	Capacitance between gate and cathode
di/dt, $(di/dt)_{cr}$	Current rate of rise, critical rate of rise of on-state current
di_G/dt	Gate current rate of rise
di_T/dt, di_F/dt	Diode/thyristor main current rate of rise
dv/dt, $(dv/dt)_{cr}$	Voltage rate of rise, critical rate of rise of off-state voltage
f	Frequency
I_D, I_T	Load current
I_{FAV}, I_{TAV}	Mean forward current
I_{FM}, I_{TM}, i_{FM}, i_{TM}	Peak forward current
I_G	Gate current
I_{GD}, I_{GT}	Gate non-trigger current, gate trigger current
I_H	Holding current
I_{ign}	Recommended trigger current (pulse transformer)
I_L	Latching current
i_R, I_{RM}	Reverse current, Peak reverse current
$I_{F(OV)}$, $I_{T(OV)}$	Overload on-state current
I_{FSM}, I_{TSM}	Surge on-state current
I_V	RMS phase current
k	Safety factor
k1	Factor
L_p	Primary inductance (pulse transformer)
L_R	Series inductance
L_s	Total load circuit inductance, Secondary inductance (pulse transformer)
L_{sp} (L_{ss})	Primary (secondary) winding stray inductance (pulse transformer)
L_σ	Stray inductance
P_{GM}, $\hat{P}_G(t_p)$	Maximum permissible gate power losses
P_R	Power losses of resistor R
Q_{rr}	Reverse recovery charge
R	Resistor, resistance

R_G, R_{GK}	Resistance of gate circuit, resistance between gate and cathode
R_p (R_s)	Winding resistances primary (secondary) winding
t_a	Arcing time (fuse)
T	Period duration
t_{gd}, t_{gr}, t_{gt}	Gate controlled delay time, gate controlled rise time, gate trigger time
t_p	Duration of trigger pulse
t_{pa}	Melting time (fuse)
t_r	Rise time of the secondary current (pulse transformer)
T_{rep}	Repetition time (pulse train)
T_{vj}, T_{vjmax}	Junction temperature, max. permissible junction temperature
V_{CC}	Driver voltage
V_D	Load voltage, forward voltage
V_{di0}	Direct output voltage (Rectifier)
V_{DRM}, V_{RRM}	Repetitive peak off-state voltage
V_{DWM}, V_{RWM}	Crest (peak) working off-state voltage
V_G	Trigger voltage
V_{GT}	Gate trigger voltage
V_{GD}	Gate non-trigger voltage
V_{GK}	Gate-cathode voltage
V_{nom}	Rated Voltage (pulse transformer)
V_p	Test voltage (pulse transformer)
V_R	Reverse voltage
V_V	RMS supply voltage (Line-Line or Line-Neutral)
V_0	Secondary voltage (pulse transformer)
V_0t	Voltage-time integral (pulse transformer)
$V_{L\sigma}$	Voltage induced by stray inductance
V_{RM}	Peak reverse voltage
V_{RSM}	Non-repetitive peak off-state voltage

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

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