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Influence of capacitive cable load on switching losses

1. Introduction

Data sheet switching losses are given for inductive load which is in accordance to the IEC requirements and a valid operation condition for most application. In small and medium power drives with long motor cables (e.g. servo drives) a substantial capacitive load has to be considered when determining switching losses. Such information is not available in the data sheet and hard to find in publications. The investigations done here are useful to give a general understanding of the topic and provide some guidance which parameter should be considered. The results are case sensitive, means the absolute values are not valid for different components and applications.
The main content and most of the figures used for this application note are based on the master thesis of Denis Richter [3] and a publication of Lars Middelstaedt [4]. Single text phrases or pictures which are taken from these publications are not identified one by one as a citation. We want to express our thanks to the authors for the investigation of the topic and for the support by Professor Andreas Lindemann from the Institute of Electrical Energy Systems of University of Magdeburg.

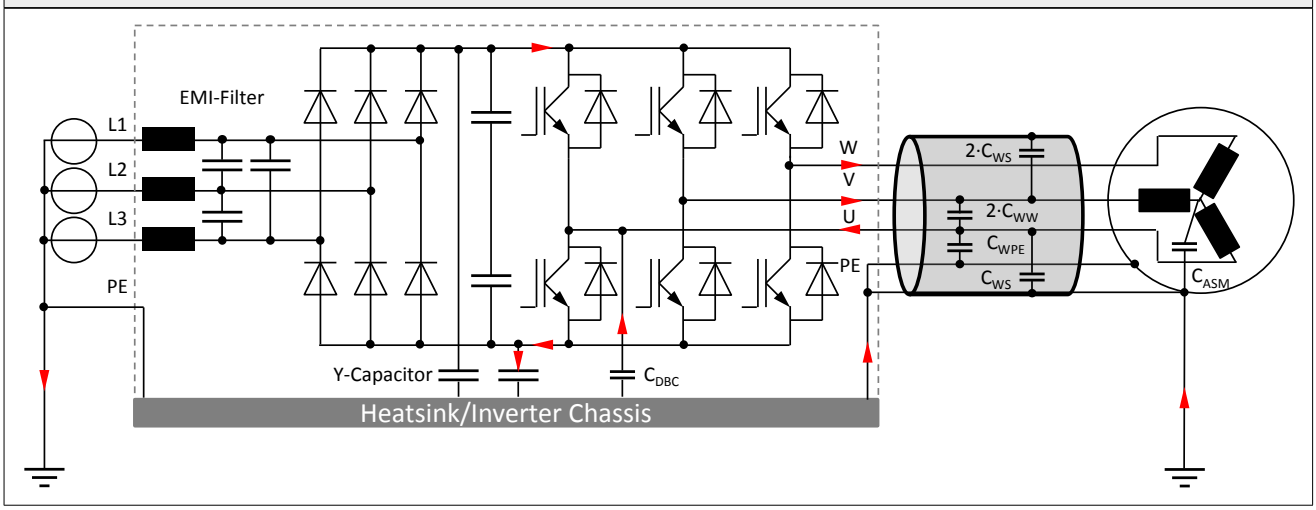
2. Measurement of switching losses

2.1 Circuit and device under test

The effect of capacitive cable load was investigated in a typical circuit for a drive application with 3 phase voltage source inverter and an asynchronous motor ASM connected via shielded cables of different length.

Figure 1 shows the principle circuit diagram with principle EMI components as line filter and Y-capacitors. IGBTs are switched with a high dv/dt between phases and from phases to ground which is causing current flow via the parasitic capacitors between wires and to shield. The arrows in Figure 1 show the current flow. The capacitive current is flowing from IGBT over Y-capacitors, chassis to cable and shield and back to DC-link and IGBT. Since the motor body is usually screwed on ground a part of current flows also direct to ground and back to grid and inverter.
The device under test is a MiniSKiiP1 (SKiiP11AC12T4V1 [1]) with nominal current $I_{C(nom)}$ = 8A and a blocking voltage V_{CES} = 1200V. The nominal switching losses are E_{on} = 0.87mJ and E_{off} = 0.75mJ → $E_{sw(ref)}$ = 1.62mJ (at 8A, 600V, 150°C, R_G=56Ω). Typical power range for this module could be a 4kW or 5.5kW Inverter.
The module is connected to a low inductive test PCB with DC-link capacitor and an interconnection to an external driver. A double shielded 4x4mm² cable [7] with a maximum current of 34 A_{rms} connects the inverter to the motor. No filter has been used at the inverter output.

Figure 1: Principle circuit diagram

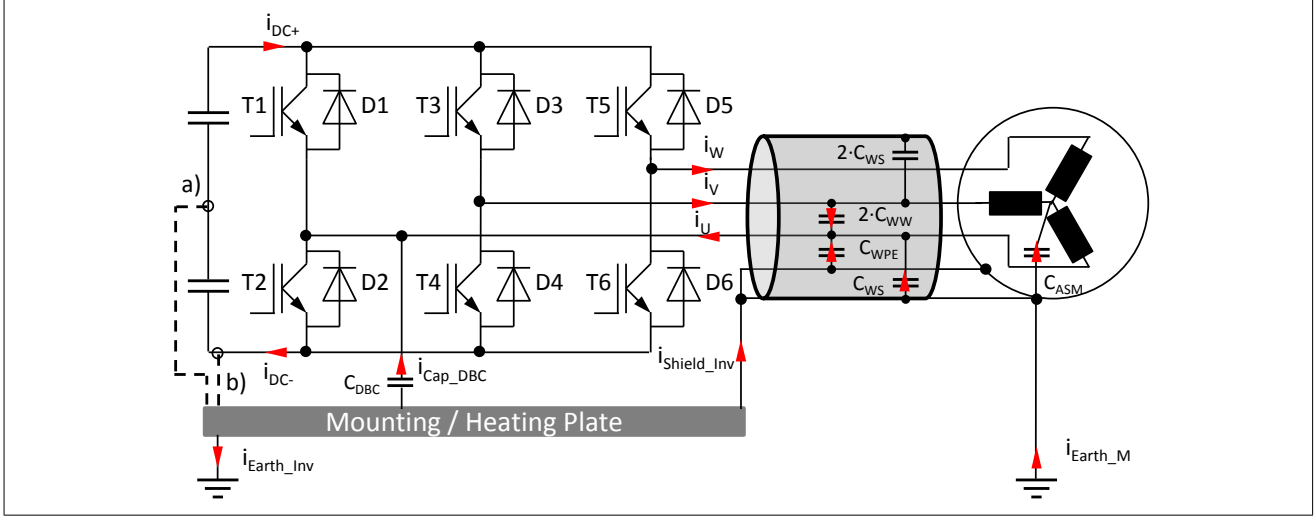


2.2 Earthing concept and coupling paths

To cover different grounding systems two different earth connections had been investigated (see Figure 2):

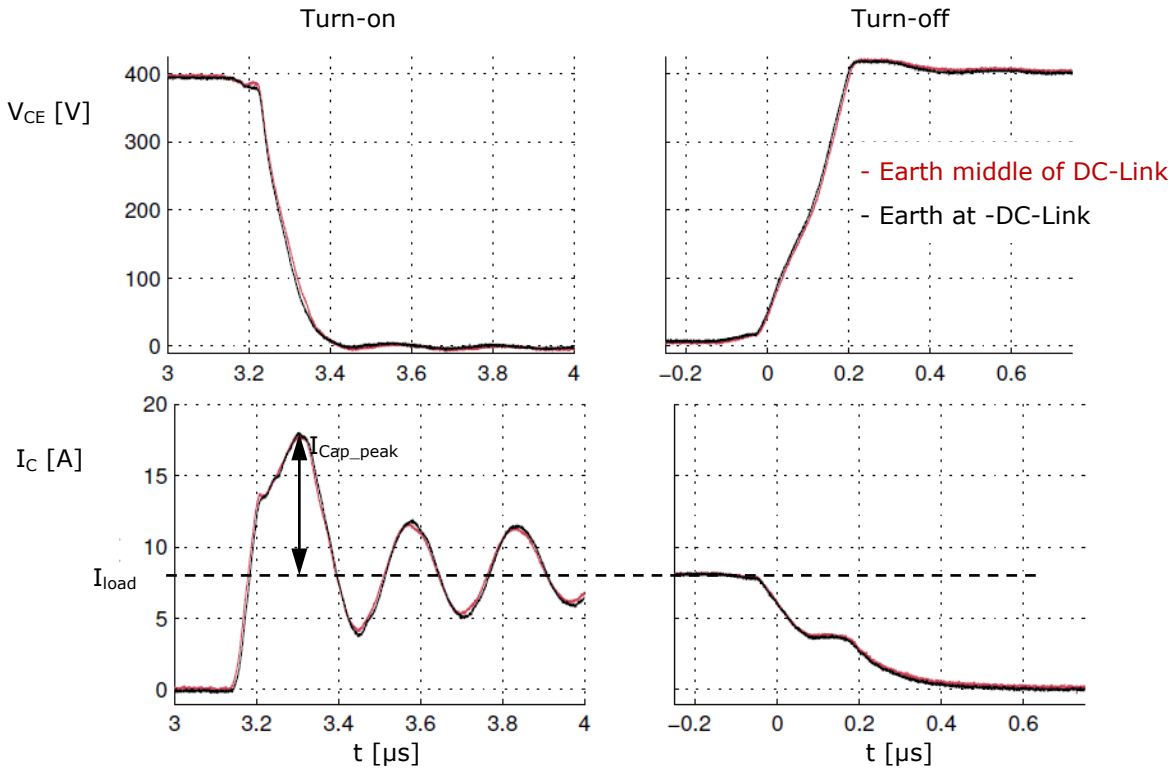
a) Earth connected in the middle of the DC link potential, which corresponds virtually to a situation with an input rectifier and an earth connected star point of the grid without Y-capacitors;
b) Earth potential on –DC, which corresponds for the BOTTOM IGBT T2 to the situation with Y-capacitors between +/-DC and earth. Since Y-capacitors have much higher value than the parasitic capacitors they are virtually like a short circuit for the HF current and don't need to be considered.

Figure 2: Earthing concepts



The earth potential is realized in the laboratory by a thick wide copper sheet underneath the complete test bench. All connections to earth from the components like modules mounting plate or motor are done with wide flexible copper stripes to realize a good low impedance contact even in the high frequency range.
An analysis of the ΔV at all coupling capacitors shows that the absolute voltage difference is the DC-Link voltage in any case, either from $-V_{CC}/2$ to $+V_{CC}/2$ or from 0 to V_{CC}. Consequently are the currents through the device identical for both concepts (Figure 3). The large DC-Link capacitor is like a short circuit for the HF capacitive coupling current. Because of easier handling for the measurement all further investigations had been done with earth potential at –DC.

Figure 3: V_{CE} and I_C of the IGBT for the two earthing concepts



The parasitic module capacitance C_{DBC} across DBC (capacitive current caused by jumping AC potential) is about 20pF for 1cm² with 0.38mm thick Al_2O_3 ceramic. The output capacitance of one IGBT is C_{oes} = 50pF. The motor cable has according to the data sheet a coupling capacitance per meter between wire and shield of C_{WS} = 150pF/m and from wire to wire of $C_{WW} = C_{WPE}$ = 90pF/m [7]. Three of the wire capacitances are in parallel, two C_{WW} from phase U to phases V and W and 1 C_{WPE} from phase U to PE wire (~270pF/m).
The wire capacitances dominate the switching behavior especially in case of long shielded motor cables. The motor capacitance C_{ASM} was not specified but its influence is at 10m cable length already relatively low, what can be seen at the only $2A_{peak}$ earth current without cable capacitances (Figure 6). Nevertheless the motor capacitance can influence the results because a small and long servo motor will have other capacitances than the used general purpose ASM.

$I_C \sim I_{-DC} = I_{shield,inv} + I_{Earth} + I_{+DC} + I_{Cap\_DBC}$

$I_{shield,inv} \sim I_{Cap\_WPE} + I_{Cap\_WS}$

$I_{+DC} = I_{load} + 2 * I_{Cap\_WW}$

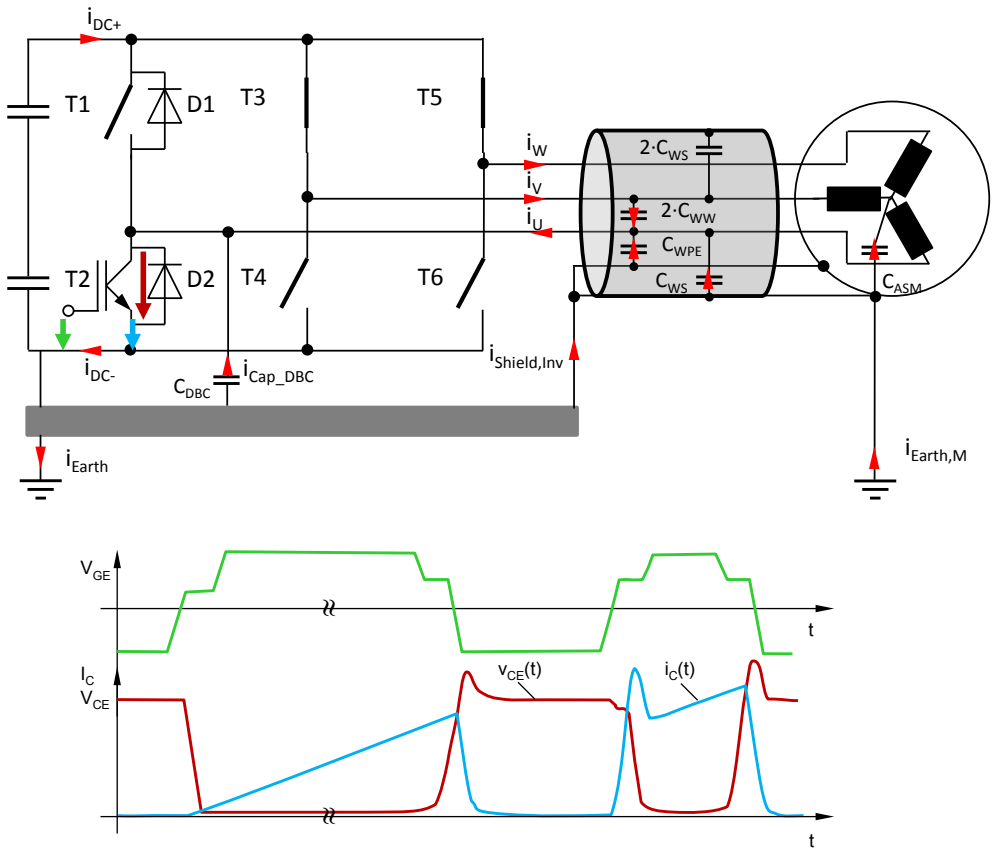
2.3 Double pulse measurement for switching losses

The Switching losses are measured according to the relevant Standard IEC60747-9 [5] in double pulse test. In difference to the standard test condition a shielded cable is connected between the power module and the inductive load. Furthermore the load is not a simple coil as normally used in the laboratory but an ASM with an additional capacitive coupling from the motor windings to the housing at earth potential. The current level is set by the pulse duration of the first pulse in a double pulse test. After turning-off the IGBT the first time a freewheeling period follows until the IGBT is turned-on the second time. The current stays

almost constant during the freewheeling period. The first turn-off and the second turn-on are used to measure the switching energy (see waveforms in Figure 4). A more detailed description for the setup and required equipment of a double pulse test can be found in [6].
The switched device is the bottom IGBT of phase U (T2) with the freewheeling diode (D1) as shown in Figure 4. The other five IGBT are either permanently switched on (T3, T6 = +DC on phase V and W) or permanently off (T1, T4 and T6).
The reference switching conditions are

- Load current $i_U = I_{C(nom)} = 8A$,
- DC-voltage $V_{CC} = 600V$,
- $T_j = 25°C$
- Driver supply voltage $V_{GG} = +15V/-7V$
- $R_G = 56\Omega$ (corresponds to the IGBT modules data sheet value)
- cable length =10m, shield at both ends connected to earth potential

Figure 4: Double pulse test configuration and principle waveform



3. Results with variation of different parameter

3.1 Cable coil or straight length

For shielded cable it does not matter how the cables are installed (straight line or on a coil). This is consequent because outside of the cable is no capacitive coupling from shield to shield and at least no changing electrical potential. The waveforms looking for both options like "reference with shield" in Figure 5.

3.2 Shielded or not shielded

Three cases had been investigated in comparison

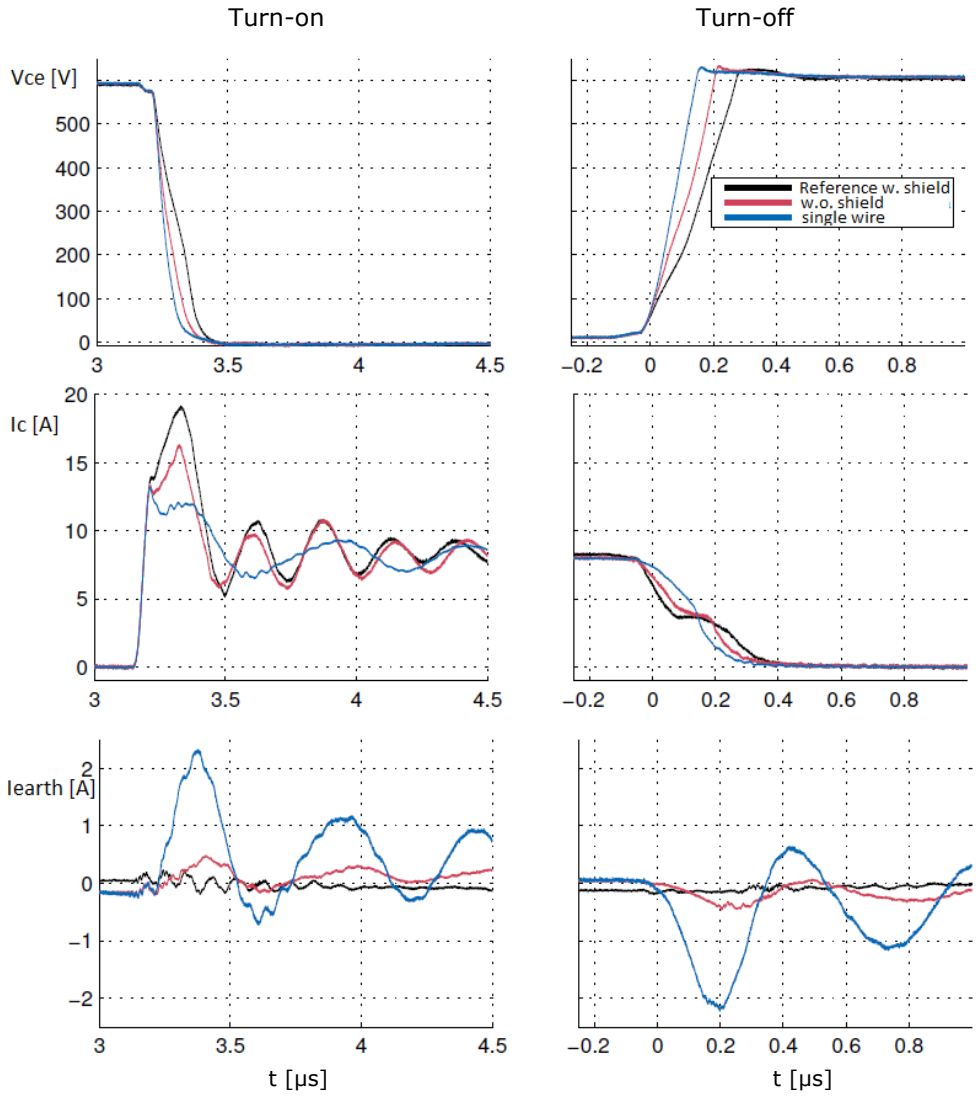
a) Reference measurement with 10m shielded cable
b) Removed shield but still twisted single wires (only coupling capacitances phase to phase, motor and power module to earth)

c) Single wires for three phases only (not twisted, only capacitances from motor and power module to earth)

By removing the shield and removing the coupling between the wires the magnitude of the capacitive current I_{Cap_peak} from 9A decreases with shield to 6.5A without shield and finally to 2A with the single wire. If the coupling in the cable disappears, than the capacitive current of the C_{ASM} can only flow via earth potential back to the inverter. In the other cases this current is flowing via shield and PE wire. If the 2A capacitive motor current are subtracted from the total capacitive current, it remains 7A for the shielded cable and 4.5A for the twisted wire. The ratio between the two currents correlates very well to the capacitive situation for the two cases, 420pF/m for the shielded cable (150pF/m +3*90pF/m) to 270pF/m for the four twisted wires.

The dv_{CE}/dt increases with less capacitive load as expected. The switching energy E_{sw} decreases from the reference point with 10m shielded cable (1.4mJ) by about 22% without shield (1.1mJ) and additional 10% for the single wire (1mJ). The single wire value of 1mJ corresponds to the value at 25°C with pure inductive load in the equipment as used for the data sheet measurements.

Figure 5: Waveforms for different cable configurations with or without shield



3.3 Cable length

The influence of the cable length had been investigated from 2m to 50m for 5 different lengths (Figure 6). At turn-on the capacitive current dominates the switching behavior. With increasing length the magnitude of the oscillating current rises. At 50m the IGBT goes even in desaturation and limits the current to about 24A (3x $I_{C(nom)}$). At the following negative swing the current crosses the zero line, the antiparallel diode

conducts and the voltage across the switch becomes negative. The oscillating part of the +DC current is caused by the coupling capacitances between the cable wires (C_{WW}). Here the reverse recovery current of the freewheeling diode is only the first small spike of $12A_{peak}$ and about 100ns duration. The difference current between I_C and I_{+DC} is caused by the capacitances to earth potential (C_{WS}, C_{WPE}, C_{DBC} C_{ASM}) of the module and cable input and flows across the modules mounting plate and also via earth potential to the motor. This additional current and partly also the slower dv_{CE}/dt increases the turn-on losses E_{on} to more than 250% compared to value without cable (see Figure 7).
At turn-off we can observe a relieved switching, because the capacitors at the output reduce the voltage rise. The main part of the capacitive current is flowing through the DC link. IGBT turn-off losses E_{off} are reduced to about 50% but the high frequency current part of I_{DC+} causes additional losses in the DC-Link capacitor. The observed step in the output voltage can be explained by some wave running effects in the cable and are independent from semiconductor switching speed or gate drive conditions. The longer the cable the more pronounced is the step. The plateau level decreases with the current and at low currents the voltage can get several plateaus.
The effect and the influence of the circuit parameter could be easily reproduced in simulation by the author of [3]. He simplified the complex network with L_W, R_W, C_{WW}, C_{WPE} and C_{WS} to a simple single wire network of 5 RLC chain elements. For cables longer than 2.5m RLC chain elements should be used instead of single lumped elements, because than it is a "long cable" with regards to the frequency range covered by the switching times of the IGBT. The RLC elements had been parametrized by the values given in the cable data sheet, with some small modifications to adapt measurement and simulation.

Figure 6: Current and voltage waveforms of the IGBT with different cable length at 25°C

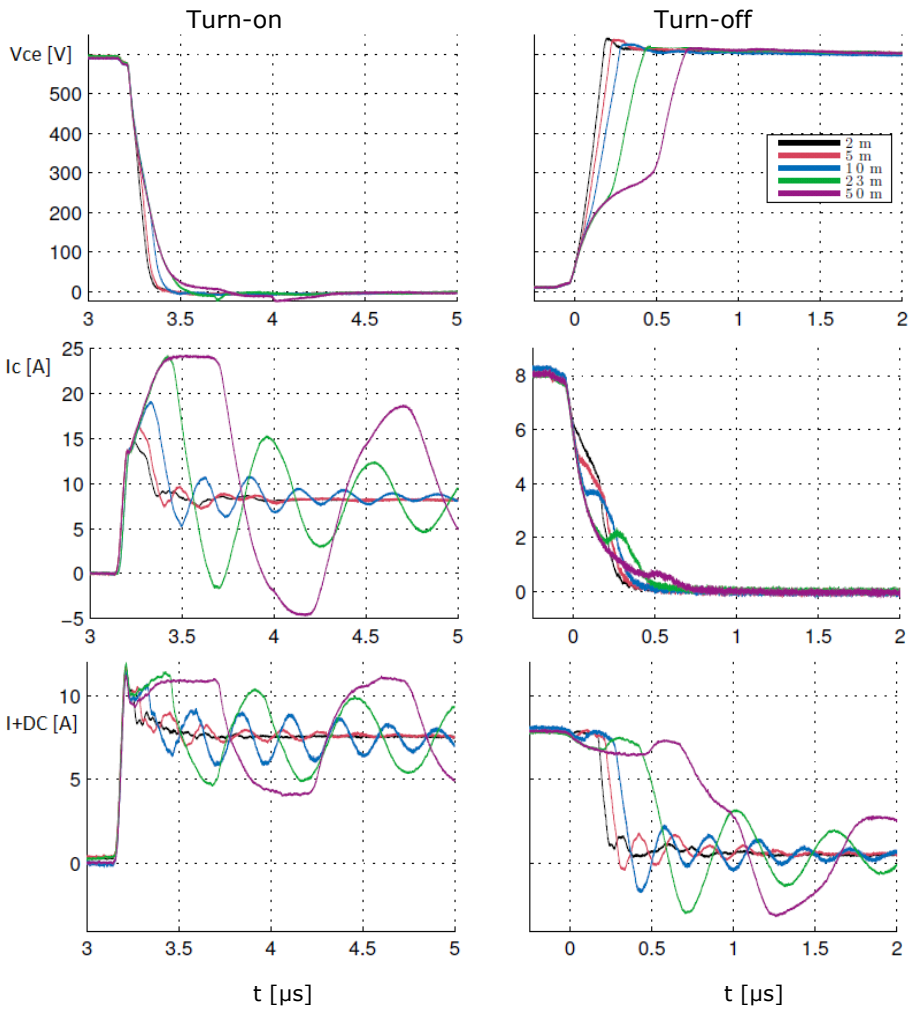
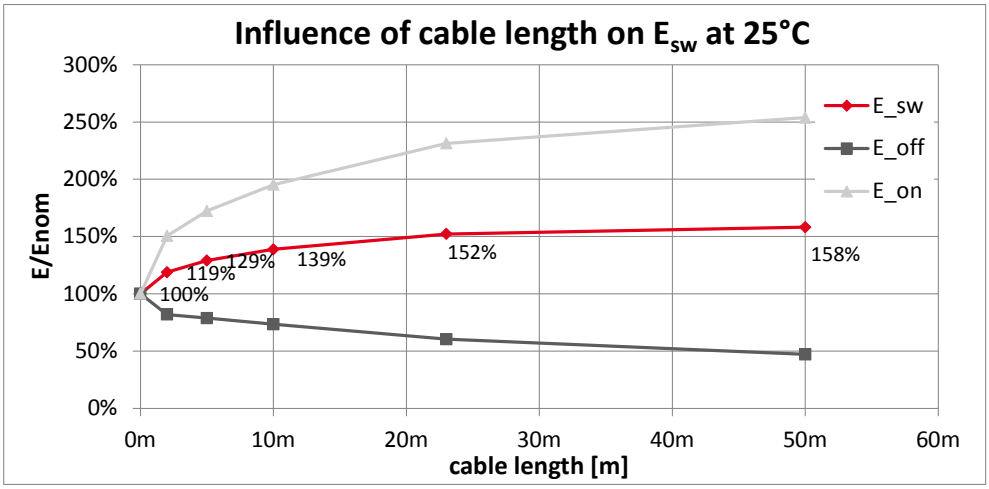


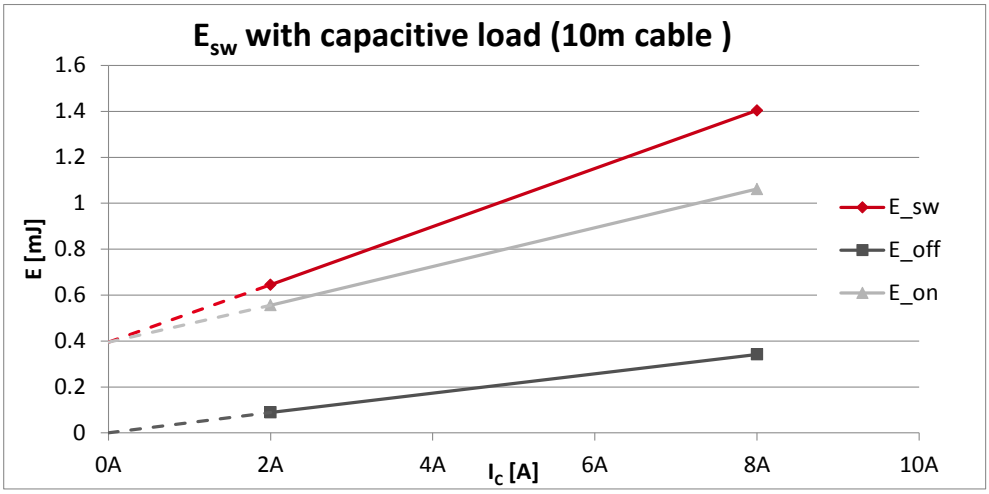
Figure 7: Switching losses as a function of cable length at rated current (8A) in relation to the pure inductive value (0m cable length) at room temperature



3.4 Load current

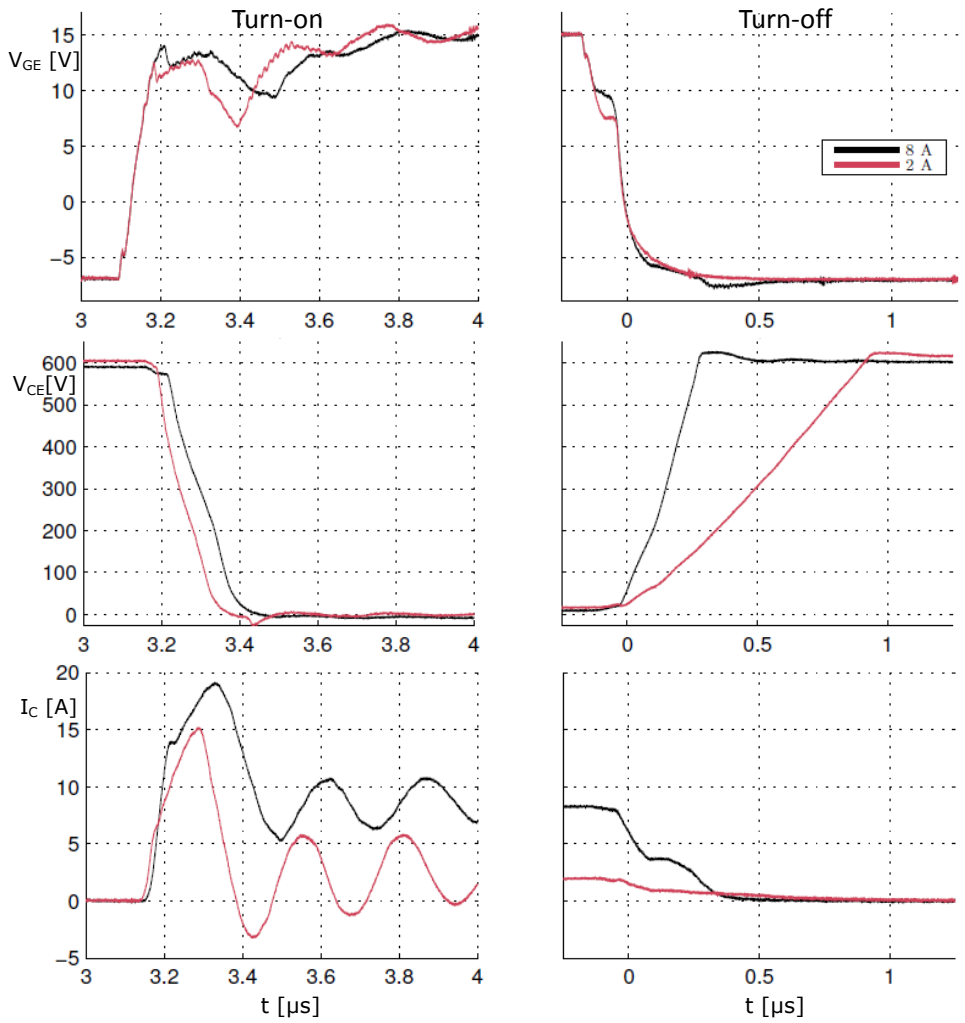
The load current level has an important influence on the turn-on losses and on the voltage rise time during turn-off. While E_{off} is zero when the current goes to zero, we can see a high offset in E_{on} at 0A (see Figure 8). The remaining 0.4mJ are about 28% of the switching losses at nominal current and T_j = 25°C. The offset on losses (absolute value) is almost constant over the complete inverter current range.
Because the semiconductor induced losses rise at high T_j and the capacitive provoked losses stay almost constant, decreases the cable effect with higher junction temperature. But there still remain about 22% of the nominal data sheet losses in idle mode at T_j = 125°C and estimated about 20% at T_j = 150°C. This additional 20% E_{sw} are used later to calculate the inverter switching losses with the influence on cable load.

Figure 8: Influence of the current level on switching losses at 25°C



In the current waveform it can be seen that the magnitude of the capacitive current (~ + 12A) is similar for the low and high load current level. For low currents the current direction changes during the oscillations and the antiparallel diode is conducting. The low current is not able to charge the capacitances parallel to the IGBT faster than with 600V/µs. Therefor the voltage raises proportional to the load current value. The effective capacitance for the configuration with 10m cable is 2µAs/600V = 3nF.

Figure 9: Waveforms at 2A and 8A I_C

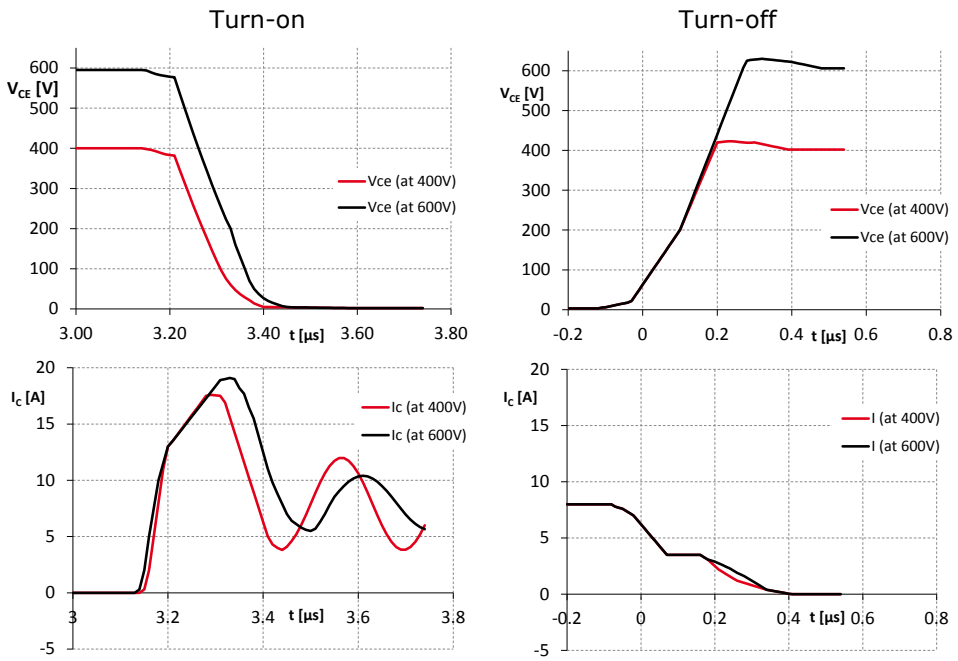


3.5 DC-Link voltage

The influence of the DC-link voltage on the switching losses is in the same range as for standard switching conditions with pure inductive load. E_{on}(400V) is about 50% of the value at 600V and E_{off}(400V) is 78% of the 600V value. The voltage exponent for the total switching energy is 1.4 as used for this IGBT technology at inductive load in general.

$$E_{sw}(400V) = E_{sw}(600V) \cdot \left(\frac{400V}{600V}\right)^{1.4}$$

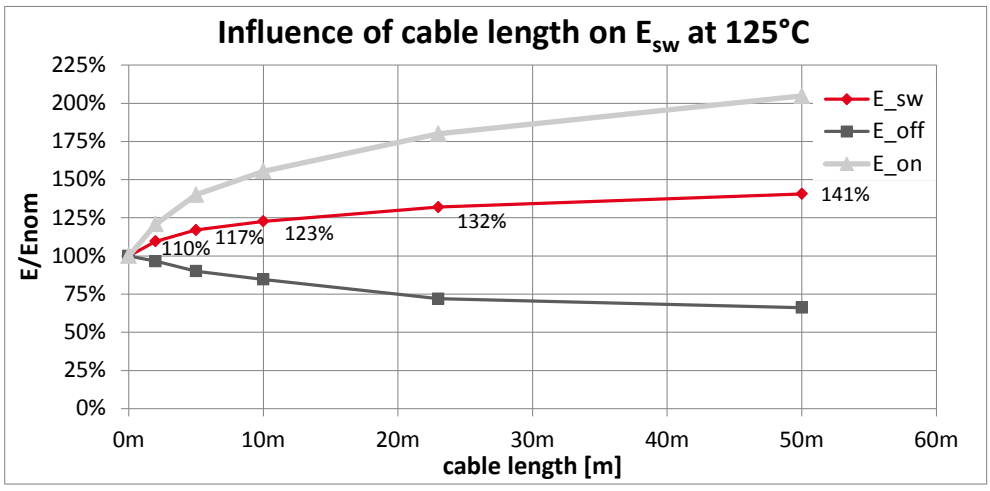
Figure 10: Waveforms with different DC-Link voltages



3.6 Junction Temperature

The chip temperature was increased passive by a heating plate to 125°C to measure the influence of the semiconductor temperature. Switching losses are measured again for different cable length.

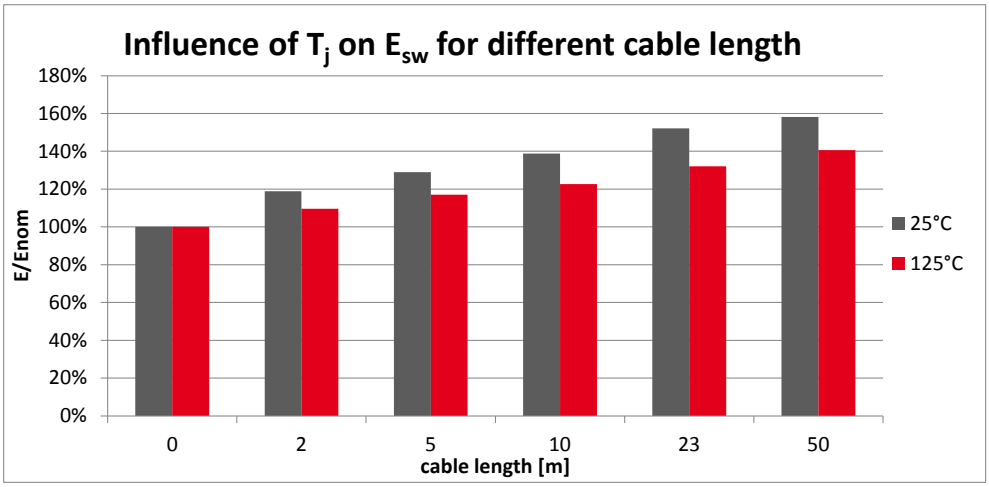
Figure 11: Switching losses as a function of cable length at rated current (8A) in relation to the pure inductive value (cable length 0m) at 125°C



For both temperatures the losses increase with longer cables. The increase of losses in percent compared to the nominal datasheet losses is lower at high temperatures as at low temperatures. Reason is that the semiconductor losses rise with higher temperatures where the capacitive part of the losses stays almost constant. Of course is the absolute value at 125°C (100% ~ 1.5mJ) higher than at 25°C (100% ~ 1mJ).
The temperature coefficient of the switching losses with 10m cable is slightly lower (0.0025/°C) compared to the data sheet condition at 0m (0.003/°C).

$$E_{sw}(T_j, 10m) = E_{sw}(125°C, 10m) \cdot \left(1 + \frac{0.0025}{°C} \cdot (T_j - 125°C)\right)$$

Figure 12: Comparison of switching losses at 25°C and 125°C @ 8A to pure inductive load (0m cable length)



Example
Estimation of switching losses at 100°C and 20m cable length, basis are the switching losses at 125°C without cable of E_{sw} = 1.5mJ.:

$$E_{sw}(125°,20m) = E_{sw}(125°C, 0m) \cdot 1.3 = 1.95mJ$$

The scaling factor "1.3" for the cable length is interpolated from Figure 12.

$$E_{sw}(100°C,20m) = E_{sw}(125°C, 20m) \cdot \left(1 + \frac{0.0025}{°C} \cdot (100°C - 125°C)\right)$$

$$E_{sw}(125°,20m) = 1.95mJ \cdot 0.94 = 1.83mJ$$

4. Consequences

4.1 Switching loss calculation

Idle mode losses are neglected in the common formula for PWM inverter switching losses [2]. These are assumed to be zero at zero current, even if that is not absolutely correct also with pure inductive load. A low capacitive current caused by the semiconductor capacitances and the modules capacitance to earth will flow in any case. The reference "ref" values used in the formula are the measurement parameter specified in the data sheet at nominal conditions, typically $T_{j(op,max)}$, $I_{C(nom)}$ and e.g. 600V for a 1200V IGBT.

$$P_{sw} = f_{sw} \cdot E_{sw(ref)} \cdot \frac{\sqrt{2} \cdot I_{out}}{\pi} \cdot \frac{1}{I_{ref}} \cdot \left(1 + TC \cdot (T_j - T_{ref})\right) \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{Exp_V}$$

It is necessary to extend the formula by an expression for the capacitive cable current. The additional expression gives an offset of switching energy (here 20% with the reference temperature of 150°C, see also 3.4) which is direct proportional to the switching frequency and is a function of cable length and applied voltage. The impact of the cable length (here "0.37") is fitted by an exponent to the increase of switching losses.

$$P_{sw} = f_{sw} \cdot E_{sw(ref)} \cdot \left(0.2 \cdot \left(\frac{l_{cable}}{10m}\right)^{0.37} + \frac{\sqrt{2} \cdot I_{out}}{\pi} \cdot \frac{1}{I_{ref}} \cdot \left(1 + TC \cdot (T_j - T_{ref})\right)\right) \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{1.4}$$

Example:
Comparison of switching losses of an PWM inverter at V_{CC} = 700V, I_{out} = 7A and f_{sw} = 8kHz, E_{sw} = 1.62mJ (8A, 600V, 150°C),

a) without cable

$$P_{sw\,a)} = 8kHz \cdot 1.62mJ \cdot \left(0.2 \cdot \left(\frac{0m}{10m}\right)^{0.37} + \frac{\sqrt{2} \cdot 7A}{\pi} \cdot \frac{1}{8A} \cdot (1 + 0.0025 \cdot (125°C - 150°C))\right) \cdot \left(\frac{700V}{600V}\right)^{1.4}$$

$$P_{sw\,a)} = 5.9W$$

b) with 20m cable

$$P_{sw\,b)} = 8kHz \cdot 1.62mJ \cdot \left(0.2 \cdot \left(\frac{20m}{10m}\right)^{0.37} + \frac{\sqrt{2} \cdot 7A}{\pi} \cdot \frac{1}{8A} \cdot (1 + 0.0025 \cdot (125°C - 150°C))\right) \cdot \left(\frac{700V}{600V}\right)^{1.4}$$

$$P_{sw\,b)} = 10.1W$$

With similar conduction losses of the IGBT at this operating condition (P_{cond} ~ 5.8W) it means that that the total losses rise from $P_{IGBT} = P_{sw} + P_{cond}$ = 11.7W without cable to 15.9W (+36%) with 20m shielded cable. Good thing is that during overload the influence in per cent goes down (e.g. 2x overload with I_{out} = 14A). The conduction losses rise to P_{cond} = 19W, while the switching losses without cable are now $P_{sw\,a)}$ = 11.9W and with 20m cable are $P_{sw\,b)}$ = 16W. Consequently raises the total losses from 30.9W to 35W (+13%).

4.2 Interlock times

Interlock or dead times are necessary to prevent a dynamic short circuit between the switches of one inverter leg. It should guarantee that one IGBT is completely turned-off before the other IGBT is turned-on. Delay, rise and fall times from the datasheet cannot be used anymore to predict a minimum interlock time with substantial capacitive load. The rise time of the voltage during turn-off at almost zero current can increase in to the µs range (see Figure 9). In that case is the minimum interlock time determined by the cable capacitances and not by the semiconductor. Neglecting that effect can cause additional losses in a bridge leg of an inverter beyond the described capacitive influence. If turning-on too early the current has not commutated to the parallel freewheeling diode, a voltage across the opposite switch is still present and the normally passive turned-on device connects two capacitances (DC-Link ↔ cable and output capacitance) with different potential. The capacitive current will cause losses in the device which is turned-on normally loss less. It is not a dynamic short circuit because the channel of the turned-off device is already closed, but the effect on the losses is similar.

4.3 Short Circuit detection

State of the art short circuit protection is a $V_{CE(sat)}$ monitoring, at which the forward voltage of the IGBT is compared with a reference voltage of typically 5…7V. In case the forward voltage exceeds the reference than the driver is set into failure mode and the IGBT will be turned off. The monitoring is activated a few µs after the turn-on command to ensure that the IGBT has reached its steady state forward voltage. The delay is called blanking time. But if the oscillation last several µs as shown in Figure 6, then the blanking time has to be increased. For actual IGBT like 4th generation of Infineon IGBT with short circuit pulse durations of t_{psc} ≤10µs it is possible to handle. The trend of chip shrinking and increasing current density at the same time reduces t_{psc} more and more for future generations of IGBT as it can be seen already today for low voltage IGBT and SiC-MOSFET. In such cases it can happen that $V_{CE(sat)}$-monitoring is not anymore possible or that unwanted error turn-off happens.

5. Conclusion

Shielded cables are often necessary to guarantee EMC requirements. The coupling capacitances of the cable increase the turn-on energy of an IGBT more than it decrease turn-off energy. Therefore in sum a high increase of the switching energy has to be considered. The increase value depends on the cable length. It can be determined in idle mode at zero current and can be added as a simple but good approach as a constant offset for the complete current range.

For higher current ratings the additional losses effect gets less important because the semiconductor induced switching losses scale almost linear with the nominal chip current (10A IGBT --> 100A IGBT: factor 10) where the cable capacitances rising by less than factor 3 for the same increase of nominal cable current capability. It cannot be specified up to which current level the shielded cable effect should be considered because it depends on maximum cable length, the ratio between switching and conduction losses and the motor operation mode (S1, S2, … S8). As long as a few single Watt per IGBT contribute remarkable to the total losses, it should be considered.

The cable capacitances have also effects on the losses in the DC link, the switching and interlock times and the blanking time of a short circuit protection with $V_{CE(sat)}$-monitoring.

Symbols and Terms

Letter Symbol	Term
ASM	Asynchronous motor or Induction motor
C_{DBC}	Capacity of a DBC copper trace carrying a chip to earth potential
C_{oes}	Small signal output capacitance of an IGBT
C_{WS}	Capacity between wire and shield per meter cable length
C_{WW}	Capacity between 2 wires per meter cable length
DBC	Direct bonded copper (ceramic), module isolator
dv/dt	Derivative of the voltage during switching, e.g. of V_{CE}
E_{on}, E_{off}, E_{sw}	Turn-on -, Turn-off -, and total switching energy $E_{sw} = E_{on} + E_{off}$
$I_{C(nom)}$	Collector current, IGBT chip nominal current
I_{CAP_xx}	Current through parasitic capacitances
i_{DC+}, i_{DC-}	Current in the DC link at + or – potential
i_{Earth}	Current between motor or mounting plate to earth potential
I_{out}	Inverter output current R.M.S
i_U, i_V, i_W	Phase current in phase U, V or W
P_{cond}	Conduction losses (of an IGBT)
P_{sw}	Switching losses (of an IGBT)
R_G	Gate resistor
T_j	Virtual junction temperature of a semiconductor
t_{pSC}	Maximum value for short circuit duration

Letter Symbol	Term
V_{CC}	Supply voltage at the DC-link
V_{CE}	Collector-Emitter Voltage
V_{CES}	Collector-Emitter Blocking Voltage, gate shorted
V_{GE}	Gate-Emitter Voltage
V_{GG}	Supply voltage at the secondary side of an IGBT driver
X_{ref}	Reference value "X" taken from the data sheet of the product

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

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IMPORTANT INFORMATION AND WARNINGS

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